Dr. Sheldon X.-D. Tan

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Education

- **Ph.D.** in Electrical and Computer Engineering, University of Iowa, Iowa City, IA, 1996-1999
- **M.Sc.** in Electrical Engineering, Fudan University, Shanghai, P.R. China, 1992-1995
- **B.S.** in Electrical Engineering, Fudan University, Shanghai, P.R. China, 1988-1992

Publication List

Dr. Sheldon Tan has published more than 220 peer-reviewed journal and conference papers. The complete publication can be found at The MSLAB publication list

Awards and Honors

- **Best Paper Award Nomination**, IEEE/ACM Asia South Pacific Design Automation Conference, Chiba, Japan, 2015. (7 out of 318 submissions, 2.2%)
- **Best Paper Award Nomination**, 51th IEEE/ACM Design Automation Conference, San Francisco, CA, 2014. (12 out of 787 submissions, 1.5%)
- **Academic Senate COR (committee on research) Fellowship**, UC Riverside, 2013.
- **Best Paper Award Nomination**, 46th IEEE/ACM Design Automation Conference, Anaheim, CA, 2009. (7 out of 682 submissions, 1%)
- **Outstanding Oversea Investigator Collaboration Award**, National Natural Science Foundation of China (NSFC), 2008.
- **Academic Senate COR (committee on research) Fellowship**, UC Riverside, 2008.
- **Best Paper Award**, IEEE Int. Conf. on Computer Design (ICCD), Lake Tahoe, CA, 2007
- **Best Paper Award Nomination**, 42th IEEE/ACM Design Automation Conference, Anaheim, CA, 2005. (16 out of 735 submissions, 2%)

- **NSF CAREER Award**, 2005.
- **UC Regent's Faculty Fellowship**, 04-05, 06-07.
- **Best Paper Award**, 36th IEEE/ACM Design Automation Conference, New Orleans, LA, 1999. (<1%)
- **First Place Poster Award** (Ph.D. Dissertation), The Annual Conference of the Center for Design of Analog-Digital Integrated Circuits (CDADIC), Seattle, WA, 1999.
- **GuangHua Fellowship** (sponsored by GuangHua Foundation), Fudan University 1993.
- **Best Graduate Student Award**, Fudan University 1992.
- **Best College Student Award**, Shanghai, China 1991.
- **Outstanding College Students Scholarships**, Fudan University, 1988-1992.

Research and Professional Experience

- **Professor**, University of California at Riverside, Riverside, CA. 07/2010 – present
- **Computer Engineering Program graduate Advisor**, University of California at Riverside, Riverside, CA. 07/2014 – 10/2015.
- **Chief Scientist and Advisor**, Shenzhen Betterlife Electronics Science and Technology, Ltd, China, 6/2013- present.
- **Co-founder, Director**, R&B Smart Devices Company Limited, China, 4/2015 – present.
- **Chair Guest Professor,** Shanghai Jiao Tong University, China, 7/2014 to present.
- **Guest Professor**, University of Electronic Science and Technology of China (UESTC), 11/2011 – present.
- **Associate Director and program co-Chair, Computer Engineer Program,** University of California at Riverside, Riverside, CA., 7/1/2009 – 7/1/2014.
- **Computer Engineering Program Undergraduate Advisor**, University of California at Riverside, Riverside, CA. 07/2011 – 07/2014.
- **Associate Professor**, University of California at Riverside, Riverside, CA. 07/2006 – 6/2010.
- **Assistant Professor**, University of California at Riverside, Riverside, CA. 07/2002 – 06/2006.
- **Guest Professor,** Shanghai Jiao Tong University, China, 04/2011 – 6/2014.
- **Visiting Professor,** Fudan University, Shanghai, China, 03/2008 – 9/2010.
- **Visiting Professor,** Tsinghua University, Beijing, China, summers of 2007 - now
- **Guest Professor,** Xi'an Institute of Post & Telecommunications, Xi'an, Shaanxi Province, China, 07/2009 - present.
- **Member of Technical Staffs**, Altera Corporation, San Jose, CA. 01/01 – 07/02.
- **Member of Technical Staffs**, Monterey Design Systems, Sunnyvale, CA. 08/99 --01/01.

- **Visiting Research Assistant**, University of Washington, Seattle, WA. 09/98 – 05/99.
- **Summer Intern**, Avant! Corp. (now Synposys), Fremont, CA. 05/98 – 09/99.
- **Summer Intern**, Rockwell Semiconductor Systems, Newport Beach, CA. 07/97 – 09/97.
- **Research Assistant**, University of Iowa, IA. 09/96 – 09/98.
- **Member of Faculty**, Fudan University, Shanghai, China. 07/95 – 08/96.

Professional Activities

Editorial Board

Existing editorial positions

- Integration, The VLSI Journal, **Editor-in-Chief**, Jan 1st, 2016 – now
- IEEE Transaction on VLSI Systems (TVLSI), **Associate Editor**, 3/2015 - now
- ACM Transaction on Design Automation of Electronic Systems (TODAES), **Associate Editor**, 3/2015 – now
- Guest editor for Special Issue on Special Issue on The 14th International Conference on Computer-Aided Design and Computer Graphics (CAD/Graphics 2015), Integration, The VLSI Journal, 2016.

Past editorial activities

- ACM Transaction on Design Automation of Electronic Systems (TODAE), Associate Editor, 2009 – 2012
- Integration, The VLSI Journal, Associate Editor, Jan. 2008 – Dec. 2015
- Guest Editor for Special Issue on "Thermal Modeling and Simulation, Thermal-Aware Design and Thermal Management for 2D/3D ICs", Integration, The VLSI Journal, 2011.
- Scientific Board, InTech Publisher, 2011-2012
- Journal of VLSI Design, Associate Editor, 2006 – 2011

Technical Program or Other Committee member or chair

- Member of technical committee member of IEEE Technical Committee on Cyber-Physical System, June 2016 -- present
- TPC Member, ACM International Symposium on Low Power Electronics and Design (ISLPED'16), San Francisco, CA, 2016.
- TPC member, International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Application to Circuit Design (SMACD), Lisbon, Portugal, July, 2016.
- TPC member, IEEE/ACM Design, Automation and Testing in Europe (DATE), D7 topic area, Dresden, Germany, March, 2016.
- Organizer and General Chair for International Workshop on Design Techniques for IoTs (ISIoT'15), Shenzhen, China, August, 2015.

- Panelist, "When Interconnect Meets Architecture: Cross-Layer Design and Optimization", 17th IEEE/ACM International Workshop on System-Level Interconnect Prediction (SLIP 2015) , June, 2015.
- TPC member, 2015 Frontier In Analog CAD Workshop (FAC), Austin, TX, Nov. 2015.
- TPC member, International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Application to Circuit Design (SMACD), Istanbul, Turkey, July, 2015.
- Committee member, ACM Outstanding PhD Dissertation Award Committee, 2015.
- TPC member, IEEE International Conference on ASIC (ASICON), Chengdu, China, Nov, 2015.
- TPC Member, ACM International Symposium on Low Power Electronics and Design (ISLPED'15), Rome, Italy, August, 2015.
- Publicity Co-Chair, The 2014 International Conference on Field-Programmable Technology (ICFPT14), Shanghai, China, Dec. 2014.
- Faculty Judge for ACM Student Research Contest, IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, CA, Nov. 2014.
- TPC Subcommittee Chair (topic 7), IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), Chiba/Tokyo, Japan, 2015.
- Regional Advisor Committee of ACM SIGDA, 2013 – present.
- TPC Member, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED'14), San Diego, CA, 2014.
- TPC member, IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, CA, 2014.
- TPC Subcommittee Chair (topic 12), IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), Singapore, Singapore, 2014.
- Faculty Judge for ACM Student Research Contest, IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, CA, Nov. 2013.
- General chair and Organizer, International Workshop on Emerging Circuits and Systems (IWECS), UESTC, Chengdu, China, 2013.
- TPC member, IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, CA, 2013.
- TPC member, IEEE International Conference on ASIC (ASICON), Shenzhen, China, 2013.
- TPC member, IEEE/ACM Design Automation Conference, (DAC), Austin, TX, 2013
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), San Jose, CA, 2013.
- TPC Subcommittee Chair (topic 12), IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), Yokohama, Japan, 2013.
- TPC member, IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, CA, 2012.
- General chair and Organizer, International Workshop on Emerging Circuits and Systems (IWECS), SJTU, Shanghai, China, 2012.
- TPC member, IEEE/ACM Design Automation Conference (DAC), San Francisco, CA, 2012
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), San Jose, CA, 2012.

- TPC Subcommittee Chair (topic 12), IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), Sydney, Australia, 2012.
- TPC member, XIIth International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Application to Circuit Design (SMACD), 2012.
- TPC member, 1st IEEE Workshop on Thermal Modeling and Management: Chips to Data Centers (TEMM), 2011.
- TPC member, IEEE/ACM Design Automation Conference, (DAC), 2011
- TPC member, IEEE International Conference on ASIC (ASICON), 2011.
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2011.
- Workshop Chair and Organizer, International Workshop on Emerging Circuits and Systems (IWECS), 2011.

- Workshop co-Chair and Organizer, International Workshop on Emerging Circuits and Systems (IWECS), 2010.
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2010.
- TPC member, IEEE International Conference on Computer Design (ICCD), 2010

- TPC member, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2009.
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2009.
- TPC member, IEEE International Conference on ASIC (ASICON), 2009.
- Workshop Chair and Organizer, International Workshop on Emerging Circuits and Systems (IWECS), 2009.

- TPC member, IEEE International Symposium on Circuits and Systems (ISCAS), 2008.
- TPC member, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2008.
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2008.

- TPC member, IEEE International Conference on Computer-Aided Design (ICCAD), 2007.
- TPC member, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2007
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2007.
- TPC member, IEEE International Symposium on Circuits and Systems (ISCAS), 2007.

- TPC member, IEEE International Conference on Computer-Aided Design (ICCAD), 2006.
- TPC member, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2006.

- TPC Member, IEEE International Behavioral Modeling and Simulation Conference (BMAS), 2006.
- TPC member, IEEE International Symposium on Quality Electronic Design, (ISQED), 2006.
- TPC member, IEEE International Symposium on Circuits and Systems (ISCAS), 2006.

- TPC subcommittee chair (topic 7), IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2005
- TPC Member, IEEE International Behavioral Modeling and Simulation Conference (BMAS), 2005.
- TPC member, IEEE International Symposium on Circuits and Systems (ISCAS), 2005.
- TPC member, IEEE International Symposium on Circuits and Systems (ISCAS), 2004.
- TPC member, IEEE Southwest Symposium on Mixed-Signal Design (SSMSD), 2003.

Conference Session Chairs

- Tutorial organizer, "Cross-Layer Reliability Aware Design, Optimization and Dynamic Management", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Chiba, Japan, Jan. 2017
- Special session organizer, "Reliability Mitigation and Resiliency-Aware Design for Energy-Efficient Systems", International Conf. on Computer-Aided Design (ICCAD'16), Austin, CA, 2016.
- Session Chair, ACM/IEEE Design Automation Conference (DAC'16), Austin, TX, 2016.
- Special session organizer, "Cross-Layer Reliability Aware Design ", IEEE/ACM Design Automation Conference (DAC), Austin, TX, June 2016.
- Session chair, IEEE/ACM Design, Automation and Testing in Europe (DATE), Dresden, Germany, March 2016.
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Macao, China, 2016.
- Session chair, Frontiers in Analog CAD (FAC), 2015, Austin, TX, Nov. 5, 2015.
- Session chair, Frontiers in Analog CAD (FAC), 2014, San Jose, CA, Nov. 2014.
- Embedded tutorial organizer, "Full-chip Electromigration Assessment and System-level EM Reliability Management" IEEE International Conference on Computer-Aided Design (ICCAD), 2014.
- Session chair, 2nd International Workshop on Cross-layer Resiliency (IWCR 2014), USC Information Science Institute (ISI), Marina del Rey, CA, July 28, 2014.
- Special session co-organizer, "Advanced battery management and applications: from smartphones to smart building", IEEE/ACM Design Automation Conference (DAC14), June 2014.
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2014.
- Session chairs, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2013.
- Session Chair, IEEE International Conference on Computer-Aided Design (ICCAD), 2012.
- Session chair, IEEE International Conference on Computer-Aided Design (ICCAD), 2011.
  Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2011.

- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2010.
- Session chair, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2009.
- Session chair, IEEE International Conference on Computer-Aided Design (ICCAD), 2008
- Session chair, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2008.
- Session chair, IEEE International Conference on Computer-Aided Design (ICCAD), 2007
- Session chair, IEEE International Symposium on Quality Electronic Design, (ISQED), 2007.
- Session chair, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2007.
- Session chair, IEEE International Conference on Computer-Aided Design (ICCAD),
- 2006
- Session chair for IEEE International Behavioral Modeling and Simulation Conference (BMAS), 2006
- Session chair, IEEE International Symposium on Quality Electronic Design, (ISQED), 2006
- Session chair, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2006.
- Session chair, IEEE/ACM Asia and South Pacific-Design Automation Conference (ASPDAC), 2005.
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC) 2000.
- Session chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2004.
- Session co-chair, IEEE International SoC Conference (SOC), 2003
- Session chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2002.

Invited Presentations:

1. **Cadence Design Systems, Inc.** San Jose, CA, "Efficient Area Optimization of VLSI Power/Ground (P/G) networks", July 16, 2002
2. **Fudan Univ.** Shanghai, China, "Area Optimization of VLSI Power/Ground Networks", Jan. 21, 2003.
3. **University of California at San Diego**, Department of Electrical and Computer Engineering, San Diego, CA, "Symbolic Analysis of Analog Circuits with Determinant Decision Diagrams", Feb. 4, 2003.
4. **Fujitsu American Research Lab**, Sunnyvale, CA, "Modeling and Simulation for Mixed-Signal System-On-a-Chip Designs", Aug. 21, 2003.
5. **The 5th International Conference on ASIC**, Beijing, China, "Circuit level alternating-direction-implicit approach to transient analysis of power distribution networks", Oct, 21, 2003.
6. **Tsinghua University,** Beijing, China, "*Fast power/ground network analysis and optimization*", Oct. 2003.
7. **Cadence Design Systems Inc.**, San Jose, CA, "Robust VLSI Power Delivery, a Verification perspective", May 05, 2004.

8. **Cadence Design Systems Inc.,** San Jose, CA, "Efficient Decap Budgeting Algorithm for Large On-Chip Power Delivery Networks", Oct. 10, 2004.
9. **Synposys Corporation Inc.**, San Jose, CA, "A General MIMO Linear Network Reduction and Realization", Oct. 11, 2004.

2005

10. **International on System-on-a-chip Workshop (ICSOC'05)**, Chengdu, China, "Efficient Decap Budgeting and Optimization", Aug. 16, 2005.
11. **Tsinghua University,** Beijing, China, "*Modeling and Simulation of Nanometer Interconnect Circuits*", Aug. 23, 2005.
12. **Cadence Design Systems, Inc.**, San Jose, CA, "Passive model order reduction and terminal reduction for interconnect circuits with multiple terminals", Nov. 9, 2005.
13. **Tessera Technologies Inc. Inc.** San Jose, CA, "Thermal issues in packaging design and fast packaging-level thermal analysis", Oct. 10, 2005.

2006

14. **University of Tokyo,** Tokyo, Japan, "Hierarchical model order reduction for wideband interconnect modeling", Jan. 25, 2006.
15. **Cadence Design Systems, Inc.**, San Jose, CA, "TermMerg: Fast terminal reduction for interconnect circuits with multiple terminals", Feb. 7, 2006.
16. **Cadence Design Systems, Inc.**, San Jose, CA, "An extended SVD-based terminal and model order reduction algorithm", June 12, 2006.
17. **Tsinghua University,** Beijing, China, "Statistical On-Chip Power Delivery Network Analysis ", Aug. 22, 2006.
18. **System LSI Design Workshop**, Fukuoka, Japan, "Recent Advance in Terminal and Model Order Reduction for Interconnect Circuits", Sept. 9, 2006.

2007

19. **Electrical Engineering Colloquium, UC Riverside, CA, "**Modeling and Simulation of Sub-90nm Interconnect Circuits: Problem, Solution and Future Challenges", May 7, 2007.
20. **Computer Science and Engineering Colloquium, UCR, "**Architecture-level thermal and power modeling and simulation for high performance microprocessor", May 21, 2007.
21. **Beijing JiaoTong University, Beijing, China,** "Modeling and analysis of 90nm VLSI Interconnects: problem, solutions and future challenges", July 5, 2007.
22. **Bejing Normal University, Beijing, China**," Architecture-level power modeling and thermal estimation for high performance microprocessor designs", July 9, 2007.
23. **Tsinghua University**, Beijing, China, "Architecture-level power modeling and thermal estimation for high performance microprocessor designs", July 18, 2007

24. **Tsinghua University**, Beijing, China, "Passive compact modeling of inductively coupled interconnect circuits by projection-based balanced truncation", July 20, 2007.
25. **Cadence Design Systems Inc, San Jose, CA,** "Passive compact modeling of inductively coupled interconnect circuits by projection-based balanced truncation", August 15, 2007.
26. **Electrical Engineering Colloquium, UC Riverside, CA, "**Architecture level power, thermal modeling, and reliable cache design for high-performance multi-core microprocessors", Oct. 22, 2007.

2008

27. **Cadence Design Systems Inc, San Jose, CA,** "Robust VLSI on-chip power delivery: challenges and solutions", January 14, 2008.
28. **Qualcomm, San Diego, CA,** "Modeling and simulation research at MSLAB at UCR", Feb. 13, 2008.
29. **Cadence Design Systems Inc, San Jose, CA,** "Numerical solution of eigenvalue problems and singular value decomposition (SVD)", March 21, 2008.
30. **Cadence Design Systems Inc, San Jose, CA,** "Parallel analysis of power grid networks on Chip-Multiprocessors", March 21, 2008.
31. **Cadence Design Systems Inc, San Jose, CA,** "Partitioning-based reduction method for large linear network analysis", June 18, 2008.
32. **Fudan Univ.** Shanghai, China, "Architecture-level Thermal Modeling and Simulation for Chip-Multiprocessor Designs", July. 10, 2008.
33. **Fuzhou Univ.** Fuzhou, China, "Thermal Behavioral Modeling and Simulation for Chip-Multiprocessor Designs", Aug. 10, 2008.
34. **Workshop of SoC Design Methodologies, National Tsing-Hua Univ.**, Tsin-Chu, Taiwan, "Efficient reduction-based methods for on-chip power grid network analysis", Sept. 9, 2008.
35. **Cadence Design Systems Inc, San Jose, CA,** "Hierarchical Reduction Based Analyses Method For Large Power Delivery Networks", Oct. 9, 2008.
36. **International Conference on Solid-State and Integrated Circuit Technology (ICSICT'08), Beijing, "**A Survey of RLCK Reduction and Simulation Methods by Fast Truncated Balanced Realization", Oct. 21, 2008.
37. **Intel Corporation, Corporation Technology Group, Hillsboro, OR, "**Architecture-level Thermal Modeling and Simulation for Multi-Core Architecture Design", Oct. 17, 2008.
38. **IBM Watson Research Center, Yorktown Height, NY, "**Variational Analysis for Large Power Delivery Networks and Full-Chip Leakage Powers of Nanometer VLSI Systems**",** Nov. 5, 2008.

2009

39. **Rice University, ECE Department, TX, "**Decentralized Model Order Reduction and Simulation of Linear Networks with Massive Ports", Jan. 29, 2009.

40. **Cadence Design Systems Inc, San Jose, CA,** "Performance Comparison for Reduction-Based P/G Network Analysis Methods", Feb 26, 2009.
41. **VirageLogic Corporation(now Synopsys), Fremont, CA, "**Boost Post-layout Verification Efficiency by Circuit Complexity Reduction", May 5, 2009.
42. **College of Engineering Seminar (CUDA Talk), UC Riverside, CA** "Parallel computing method for on-chip power grid analysis based on the multi-core computing platforms", June 2, 2009.
43. **Shanghai Jiao Tong University, School of Microelectronics, Shanghai, China, "**Variational Analysis of Full-Chip Leakage Power in Nanometer VLSI Systems**",** June 16, 2009.
44. **Yunnan University, Information School**, **Kunming, China**, "Chip-Level Thermal Characterization for Multi-Core Microprocessor Design", June 25, 2009.
45. **International Workshop on Emerging Circuits and Systems (IWECS'09), Shanghai, China, "**Chip-Level parameterized thermal modeling for multi-core microprocessor design", July 6, 2009**.**
46. **International Workshop on Emerging Circuits and Systems (IWECS'09), Shanghai, China, "**Opening Speech for IWECS'09", July 6, 2009
47. **Xi'an Institute of Post & Telecommunications, Dept of Computer Science, Xi'an, Shaanxi Province, China**, "Variational Analysis of Clock Networks Considering Environmental Uncertainty", July 8, 2009.
48. **Xi'an Jiao Tong University, Dept of Electrical Engineering, Xi'an, Shaanxi Province, China**, "Variational Analysis of Clock Networks Considering Environmental Uncertainty", July 10, 2009.
49. **CEC Huada Electronic Design Co., Ltd, Beijing, China,** "Boost Post-layout Verification Efficiency for Analog Circuits by Compact Modeling of Parasitics", July 24, 2009.
50. **The 5th International Conference on ASIC**, Beijing, China, "Architecture level thermal modeling for multi-core systems using subspace system method", in Changsha, China, Oct, 2009.

2010

51. **2nd Nanoelectronics and Advanced Design Seminar at INAOE (Institute National Astrophysics, Optical and Electrics) at Puebla, Mexico ,** "Architecture-level Thermal Modeling and Simulation for Multi-Core Chip Design", May 21, 2010.
52. **Fudan Univ. Shanghai, China**, "Statistical Analysis of Full-Chip Leakage Power in Nanometer VLSI Systems", July. 23, 2010.
53. **International Workshop on Emerging Circuits and Systems (IWECS'10), Hefei, Anhui Province, China, "**Composable Thermal Modeling for Multicore Microprocessor Design", August 5, 2010.
54. **University of Electronic Science and Technology of China (UESTC), Chengdu, China,** "Thermal Modeling and Estimation for Multi-Core Microprocessor Design", August 10, 2010.

55. **Intel Corp. Chandler, AZ, ATTD Group**, "Chip-Level Thermal Modeling and Characterizations for Single and Multi Core Processor Designs", Sept. 13, 2010.
56. **International Conference on Solid-State and Integrated Circuit Technology (ICSICT'10), Beijing, "**UiMOR -- UC Riverside Model Order Reduction Tool for Post-Layout Wideband Interconnect Modeling", Nov. 4, 2010.

2011

57. **Shanghai Jiao Tong University, School of Microelectronics**, Shanghai, China, "Performance bound analysis of analog circuits considering process variation", May 30, 2011.
58. **Cisco System Corporation, San Jose, CA**, "Thermal Modeling and Simulation Research for High-Performance Package and Chip Design", June 14, 2011.
59. **Tsinghua University, Microelectronic Institute, Beijing, China,** "Thermal Modeling and Estimation for High-Performance Package and Chip Design", July 12, 2011.
60. **International Workshop on Emerging Circuits and Systems (IWECS'11), Hangzhou, Zhejiang Provence, China,** ""Graph-based Parallel and Statistical Analysis of Large Analog Circuits Based on GPU Platforms, August 4, 2011.
61. **Nanyang Technological University, School of Electrical and Electronic Engineering, Singapore, Singapore** , "Thermal Modeling, Estimation and Prediction for Package Design and On-Chip Temperature Regulation",. Aug. 16, 2011.
62. **The Hong Kong University of Science and Technology, Department of Electrical and Computer Engineering, Hong Kong, China,** "Reliable Thermal Estimation and Prediction for On-Chip Temperature Regulation", Aug. 22, 2011.
63. **The University of Hong Kong, Department of Electrical and Electronic Engineering, Hong Kong, China**, "Graph-based Parallel and Statistical Analysis of Analog Circuits Based on GPU Platforms", Hong Kong, Aug. 23, 2011.
64. **The EDA workshop, Department of Electrical Engineering, National Taiwan University, Taiwan**, "Performance Bound Analysis for Analog Circuits Under Process Variations", Sept 10, 2011.
65. **Mentor Graphics Corp, Calibre Group, Fremont, CA,** "Thermal Modeling and Analysis Research for High-Performance Package and Chip Design", Dec. 14, 2011.

2012

66. **Shanghai Jiaotong University, School of Microelectronics, Shanghai, China,** "Graph-based Parallel and Statistical Analysis of Analog Circuits on GPU Platforms", April 26, 2012
67. **MediaTek Singapore Pte Ltd, Singapore**, "Thermal Analysis and Runtime Management Research for Multi-core Microprocessors", July 27, 2012.

68. **International Talent Innovation and Entrepreneurship Week of Shanghai, 2012, Shanghai**, "New Battery State of Charge Estimation Techniques for EV", Aug. 7, 2012.

69. **International Workshop on Emerging Circuits and Systems (IWECS'12), Shanghai Jiao Tong University, Shanghai, China**, "Parallel Computing and Simulation for VLSI systems", Aug. 9, 2012.

2013

70. **INAOE (Institute National Astrophysics, Optical and Electrics), Department of Electrical Engineering, Puebla, Mexico ,** "Fast GPU-accelerated sparse matrix-vector multiplication (SpMV)", May 3, 2013.

71. **International Workshop on Emerging Circuits and Systems (IWECS'13), University of Electronic Science and Technology of China (UESTC), Chengdu, Sichuan Province, China**, "Thermal resistance modeling and characterization for TSV and TSV array", July 26, 2013.

72. **Seoul National University, Embedded System Research Center (ESRC), Seoul, Korea,** "Architecture Level Thermal Modeling, Management for Multi-core and 3D Microprocessors", Dec. 10, 2013. Host: Prof. Naehyuck Chang of SNU.

2014

73. **The University of Hong Kong, Department of Electrical and Electronic Engineering, Hong Kong, China**, "New More Physics-Based Full-Chip Electron-migration Modeling and Analysis", Jan. 24, 2014. Host: Prof. Ngai Wong of Univ. of HK.

74. **The University of California at San Diego, Department of Electrical and Computer Engineering, San Diego, CA.** "New Physics-Based Full-Chip Electron-Migration Analysis and System-level Reliability Management", April 23, 2014. Host: Prof. Chung-Kuan Cheng of UCSD.

75. **The Institute of Computing Technologies, State Key Lab of Computer Architecture, Chinese Academy of Science, Beijing, China,** "Physics-Based Full-Chip Electron-Migration Analysis and System-level Reliability Management", July 4th, 2014. Host: Prof. Yu Hu of ICT, CAS.

76. **2nd International Workshop on Cross-layer Resiliency (IWCR 2014), USC Information Science Institute (ISI), Marina del Rey, CA**, "Physics-Based Full-Chip Electron-Migration Modeling and System-level Reliability Management", July 28, 2014.

77. **EDA workshop, Daejeon Convention Center, Daejeon, Korea**, "Physics-Based Full-Chip Electron-Migration Modeling and Cross-Layer Reliability Management", August 26, 2014.

78. **University of Electronic Science and Technology of China (UESTC), School of Microelectronics and Solid State Electronics, Chengdu, China,** "Physics-Based Full-Chip Electron-Migration Modeling and Cross-Layer Reliability Management", Sept. 10, 2014.

79. **13th International Workshop on Stress-Induced Phenomena in Microelectronics (Stress Workshop), The University of Texas at**

Austin, Austin, "Physics-Based Electromigration Assessment for Power Grid Networks", Oct. 15th, 2014.,

80. **IEEE/ACM International Conference on Computer-Aided Design (ICCAD'14), Austin, TX,** "Lifetime optimization for real-time embedded systems considering electromigration effects", Nov. 13, 2014. (invited talk)
81. **Guowei Microelectronic Corp., Shenzhen, China,** "Reliability Analysis and Optimization for VLSI and FPGA Systems", Dec. 14, 2014.

2015

82. **International Symposium on Design Technologies for IoT (ISIoT'15), HIT, Shenzhen, China, "**Compact Thermal Modeling for Energy-Efficient Smart Building Management", August 14, 2015.
83. **1st US-China Internet Plus and Innovation and Entrepreneurship Resource Summit (Mobile Storage, Sensing the world), Hangzhou, China**, "Smart Hub and Device for Smart Education", August 26, 2015.
84. **SRC e-workshop (GRC CADT-System, Logic & Physical Design),** "Thermal-Sensitive System-Level Reliability Analysis and Management for Multi-Core and 3D Microprocessors", Sept. 29, 2015. Host: Dr. Bill Joyner.
85. **IEEE/ACM International Conference on Computer-Aided Design (ICCAD'15), Austin, TX, "**Learning based compact thermal modeling for energy-efficient smart building management", Nov. 13, 2015. (invited talk)
86. **ShanghaiTech University**, **School of Information Science**, **Shanghai, China**, "Physics-Based Electron-migration Modeling and Cross-Layer Reliability Management", Nov. 25, 2015. Host: Prof. Pingqiang Zhou.

2016

87. **IEEE/ACM, Asia South Pacific Design Automation Conference (ASP-DAC'16),** "Thermal modeling for energy-efficient smart building with advanced overfitting mitigation technique", January 24, 2016. Macao, China (invited talk)
88. **Technical University Munich, Munich, Germany (as part of the EDA workshop)**, "Learning-Based Dynamic Reliability Management For Dark Silicon Processors", March 18, 25, 2016. Host: Prof. Ulf Schlichtmann and Prof. Helmut Graeb.
89. **Karlsruhe Institute of Technology (KIT)**, **Institut für Technische Informatik (ITEC), "**Physics-Based Electron-migration Assessment and Cross-Layer Reliability Management", June 2nd, 2016. Host: Prof. Mehdi Tahoori.
90. **13th International Workshop on Stress-Induced Phenomena in Microelectronics (Stress Workshop), Bad Schandau, Germany**, "EM Modeling and Recovery Analysis under Time-Dependent Current and Temperature Stressing", May 30, 2016. (poster)
91. **ACM/IEEE Design Automation Conference (DAC'16),** Austin, TX, "Cross-layer modeling and optimization for electromigration induced reliability",June 7, 2016. (Invited talk).

92. **4nd International Workshop on Cross-layer Resiliency (IWCR 2016), University of California at Irvine**, "Voltage-based EM Immortality Check and new EM Signoff Flow", July 26, 2016.

Tutorial and Invited Talks in Special Session Presentations:

- Paul M. Harvey, Howard Chen, Chung-Kuan Cheng, Manjid Borah, Lei He, and Sheldon Tan, "High Performance Interconnect and Packaging", full day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference*, January 24, 2006.
- Sheldon X.-D. Tan, Jeffrey Fan, "Inductance Extraction and Compact Modeling of Inductively Coupled Interconnects in the Presence of Process Variations", half-day tutorial*, ASICON'07*, Oct. 2007, Guilin, China (invited).
- Sheldon X.-D. Tan, "Advanced modeling and analysis techniques for nanometer interconnect and multi-core VLSI circuits", *ASIC & System Lab, Fudan University, July 27 to Aug. 1, 2008*. (Four presentations were given in the short course), Shanghai, China.
- Sheldon X.-D. Tan and Hai Wang, "Architecture Level Thermal Modeling, Prediction and Management for Multi-core and 3D Microprocessors", half day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference* (ASPDAC14), Singapore, Singapore, January 20, 2014.
- Valeriy Sukharev, Sheldon Tan, Marko Chew, "Full-chip Electromigration Assessment and System-level EM Reliability Management", embedded tutorial, IEEE/ACM International Conference on Computer-Aided Design (ICCAD14), Nov. 2014.
- Sheldon Tan, Medhi Tahoori, Haibao Chen, "Cross-Layer Reliability Aware Design, Optimization and Dynamic Management", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Chiba, Japan, Jan. 2017

Review activities:

Research Proposals

- UC MICRO 2005 (two proposals).
- UC MICRO 2006 (three proposals)
- NSF , 2007, (two proposals), 2008 (one proposal), 2009 (one proposal)
- One NSF Panel, 2016 (15 proposals).

Journals

- IEEE Transaction of Computer-Aided Design of Integrated Systems (TCAD), 2002-present.

- IEEE Transaction of Circuit and Systems I, (TCAS-I), 2002-present.
- IEEE Transaction of Circuit and Systems II, (TCAS-II), 2002-present.
- Integration, The VLSI Journal, 2002-present.
- IEEE Transaction on Very Large Scale Integrated Systems (TVLSI), 2006 – present.
- ACM Transaction of Design Automation of Electronic Systems (TODAES), 2001-present.
- International Journal of Circuit Theory and Application, 2006 – present.

Conferences

- IEEE Asia and South Pacific Design Automation Conferences (ASPDAC), 2005, 2006,2007, 2008.
- IEEE International Modeling and Simulation Conference (BMAS), 2005- present.
- International Symposium on High-Performance Computer Architecture (HPCA), 2005
- IEEE International Symposium on Circuits and Systems (ISCAS), 2002,2004 – 2008.
- IEEE/DAC Design Automation Conference (DAC), 2000-now.
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 1999, 2000, 2006, 2007
- IEEE International Conference on Computer Design (ICCD), 2005 – present.
- IEEE International Symposium on Quality Electronic Design (ISQED), 2005 – present.

Professional society memberships

- **Senior Member**, the Institute of Electrical and Electronics Engineers (1997-present)
- Member, Society of Industry and Applied Mathematics (SIAM) (2008-2009)
- Consultant for Cadence Design Systems, Inc. San Jose, CA. Aug. 2003 to Aug. 2004

Patent disclosures:

- Sheldon X.-D. Tan, X. Wang, B.A. Fairbanks, "I/O Pin Placement Algorithm For Programmable Logic Devices" Filed on May, 2003. U.S. Patent No. 7111265 (USA) (approved on 9/19/2006).

- Sheldon X.-D. Tan, B. Yan, "Decentralized complexity reduction of parasitic interconnect circuits", UC Case No. 2008-783-1, US provisional patent. (filed on May 28, 2008)

- Sheldon X.-D. Tan, D. Li, "Extended truncated balanced realization method for on-chip power grid network analysis", UC Case No. 2008-784-1, US provisional patent. (filed on Feb. 27, 2008).

- X. Hong, Y, Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, "Transient analysis of on-chip power grid networks based on equivalent circuits", Patent No. ZL 03104770.X (China)

- X. Hong, Y, Cai, J. Fu, Y. Luo, Z. Pan, Sheldon X.-D. Tan, "Fast decap allocation method for noise reduction in the on-chip power grid networks", Patent No. ZL031570526 (China)

- X. Hong, Y, Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, "Relaxed hierarchical transient analysis method for power grid networks", Patent No. ZL 200510011804.2 (China)

- K. He, X. Huang, Sheldon X.-D. Tan, "EM-Based on-Chip Aging Sensor for Detection and Prevention of Recycled ICs", Sept. 24, 2015. US provisional patent, UC case: 2016-182-1.

- K. He, X. Xie, Sheldon X.-D. Tan, "Multi-functional on-chip sensor and the post-authentication policy for comprehensive detection of counterfeited ICs", Dec. 12, 2015, US provisional patent, UC case: 2016-357-1

Other Services

Department and University Services

- UCR EE Faculty Search Committee, member (July 2002 to July 2003)
- UCR EE Faculty Search Committee, member (July 2003 to July 2004)
- UCR EE Faculty Search Committee, member, (July 2004 to July 2005)
- UCR EE Computing Committee, **Chair**, (April 2005 to June, 2006)
- UCR International Education Committee, member, (April 2005 to July 2006)
- Cooperating Faculty Member, Department of Computer Science and Engineering, (July 2003 to present)
- EE ABET Accreditation Committee, member, (April 2006 to June 2006)
- UCR EE Faculty Search Committee, **Chair**, (July 2006 to July 2007)
- UCR EE Graduate Committee, member, (July, 2006 to June 2007)
- UCR EE Chair Committee, member (July, 2006 to June 2007)
- UCR ECE Ad Hoc Committees (July, 2006 to present)
- UCR EE Undergraduate Committee, Member (July 2007 to present)

- BCOE, Computer Engineering Program Committee, **Co-Chair**, (Jan. 2008 – June, 2009).
- UCR Campus-level Senate **Committee on Committee (CoC)**, **member**, (July 2009 to June 2012)
- UCR EE, Committee on External Relations and Development, member (July 2009 – 2011)
- BCOE, Computer Engineering Program, **Associate Director** (July 2009 – 2013)
- BCOE, Computer Engineering Program, **Undergraduate advisor**, (Oct, 2009 – June 2014)
- UCR EE, Faculty Search Committee, **Chair**, (July 2010 to June 2011)
- UCR EE, Colloquium Organizer and Host, (Jan, 2011 to June 2011)
- BCOE, Executive committee, **member**, (July, 2012 – March 2014)
- UCR, member of the Search Committee for Vice Provost for International Affairs (VPIA), Feb. 2014 to July 2014.
- BCOE, Computer Engineering Program, **Graduate Advisor** (July 2014 – Sept 2015)
- UCR ECE, Ad Hoc Committee (member, Oct, 2015).

Outreach Activities

- Judge for RUSD (Riverside Unified School District) Sence Fair, March 11, 2003.
- Mentoring for Computer Engineering students, Sept. 2004 – January 2005.
- Mentoring for Computer Engineering students, Jan 2005 – March 2005.
- Mentoring for Computer Engineering students, Fall 2005 – January 2006.
- Representing EE Department as the faculty for Chancellor's Welcome for new freshman students, Feb. 2, 2006.

Research Awards and Grants (more than $4.3 millions):

1. **University of California Academic Senate Research Fund**, "Symbolic Modeling of Analog Circuits and Deep Submicron VLSI Interconnect", $16,00, July, 2003 to June 2004. PI.

2. **Semiconductor Research Corporation CSR program,** (No.2003-HJ-1046G), "Warp Processor", $48,000, July, 2003 to June 2005. co-PI (PI Prof. Vahid).

3. **Cadence Design Systems**, "Fast On-Chip Transistor Level Power/Ground Dynamic Grid Analysis", $20,000, Sept. 2003 to Aug. 2004. PI (as consultant).

4. **University of California Academic Senate Research Fund**, "Behavioral Models for Mixed-Signal and Radio-Frequency Integrated Circuits", $2032, July, 2004 to June 2005. PI.

5. **UC Regent's Faculty Fellowship**, "Wideband Behavioral Modeling of Mixed-Signal and RF Circuits", $24,00, July, 2004 to June 2005. PI.

6. **Cadence Design Systems**, "Fast Decap Budgeting for Robust On-Chip Power Delivery Networks", $10,000, Sept. 2004 to Aug. 2005. PI.

7. **UC MICRO program** (via Cadence Design System) (#04-088), "Decoupling Capacitance Budgeting for Robust On-Chip Power Delivery Networks", $7294, Sept. 2004 to Aug. 2005. PI.

8. **University of California Academic Senate Research Fund**, "Fast Thermal Analysis For Dynamic Thermal Management of Nanometer VLSI Systems", $1920, July, 2005 to June 2006. PI.

9. **National Science Foundation CAREER Award** (CCF-0448534), "CAREER: Career Development Plan: Behavioral Modeling, Simulation and Optimization for Mixed-Signal SoCs ", $400,000, June 2005 to May 2010. PI.

10. **National Science Foundation Supplemental REU** (CCF-0529754), $6000, June 2005 to June 2006. PI.

11. **Semiconductor Industry Association (SIA) Stay Tech Program (SST)**, "Enhancing Undergraduate Student Retention For Computer Engineering Education in the University of California at Riverside", $20,000, Sept. 2005 to Aug. 2006. PI (co-PI Prof. Vahid).

12. **National Science Foundation, Office of International Science and Engineering (OISE)**: (OISE-0451688), "U.S.-China Planning Visit: Development of Computer-Aided Design (CAD) Tools for Physical Design and Verification of Low Power Nanometer VLSI Design", $10,890, May 2005 – April. 2007. PI.

13. **UC MICRO Program** (via Cadente Design System Inc.) (#05-111), "Combined Multi-Input Multi-Output Model Order Reduction and Topology Reduction for High-Performance VLSI Systems ", $31,103, Sept. 2005 to Aug. 2006, PI.

14. **National Science Foundation, CISE/CCF** (CCF- 0541456), **"**Fast Software Thermal Sensing and Control for Efficient Dynamic Thermal Management", $275,000, co-PI, (PI: J. Yang, co-PI: J. Chen), June, 2006 to May, 2009.

15. **University of California Academic Senate Research Fund**, "Statistical Simulation and Modeling Methods for Nanometer VLSI Circuits", $1929, July, 2006 to June 2007. PI.

16. **National Science Foundation, Office of International Science and Engineering (OISE):** (OISE-0623038), "IRES: Development of Global Scientists by Research Collaborations on Simulation and Optimization of Nanometer Integrated Systems", $150,000, May 1, 2007 to April 30, 2010, PI.

17. **UC Regent's Faculty Fellowship/Faculty Development Award**, "Statistical Simulation and Modeling for Nanometer VLSI Designs", $3500, July, 2006 to June 2007. PI.

18. **UC MICRO Program** (via Cadence Design System Inc.) (#06-252), "Bahavioral and compact modeling of mixed-signal and RF circuits", $32,250, Sept. 2006 to Aug. 2007, PI.

19. **Semiconductor Industry Association (SIA) Stay Tech Program (SST) (extended for second year)**, "Enhancing Undergraduate Student Retention For Computer Engineering Education in the University of California at Riverside", $15,000, Sept. 2006 to Aug. 2007. PI (co-PI Prof. Vahid).

20. **Verizon Electrical Engineering Fellowship,** $6000, 1/1/2007 to 12/31/2007, PI (co-PI Prof. Vahid).

21. **University of California Academic Senate Research Fund**, "Variational Analysis for Nanometer Interconnect Circuits", $1711, July, 2007 to June 2008. PI.

22. **National Science Foundation Supplemental REU** (CCF-0731962), $6000, July 2007 to August 2008. PI.

23. **UC MICRO Program** (via Intel Corporation) (#07-101), "Parameterized Thermal Behavioral Modeling and Simulation for Designing System Platforms", $90,000, Sept. 2007 to Aug. 2008, PI.

24. **UC MICRO Program** (via Cadence Design System Inc.) (#07-105), "Compact Modeling Techniques for Inductively Coupled Interconnect Circuits.", $26, 696, Sept. 2007 to Aug. 2008, PI.

25. **University of California Academic Senate Research Fund**, "Statistical Model and Simulation for VLSI Design", $1400, July, 2008 to June 2009. PI.

26. **COR (committee on research) Research Fellowships**, "Statistical Characterization of High-Speed Interconnects in Nanometer VLSI Systems", $5000, July, 2008 to June 2009. PI.

27. **National Science Foundation Supplemental REU** (CCF- 0830304), $6000, June 2008 to June 2009. PI.

28. **National Natural Science Foundation of China (NSFC), Outstanding Oversea Investigator Collaboration Award** (杰青-B), (60828008/ F040204), "Variation-Aware Design Technologies for Nanometer VLSI System", $30,800, (200,000RMB), Phase-I, Jan., 2009 to Dec. 2010, PI. Co-PI: Yici Cai.

29. **Fudan University**, Nanoelectronic innovation platform for visiting scholar program, $5000, Jun, 2008 to May/2010.

30. **UC MICRO Program** (via Intel Corporation) (#08-11), "Parameterized Thermal Behavioral Modeling and Simulation for Designing System Platforms", $58,500, Sept. 2008 to Dec. 2009, PI.

31. **UC MICRO Program** (via Cadence Design System Inc.) (#08-12), "Parallel computing for robust on-chip power delivery based on chip-multiprocessing", $23,400, Sept. 2008 to Dec. 2009, PI.

32. **National Science Foundation, NSF/SRC Multi-core Program (**CCF-0902885), "Parameterized Architecture-Level Thermal Modeling and Characterization for Multi-Core Microprocessor Design", $259,544.40, Aug. 1, 2009 to July 30, 2012. PI, Co-PI: Yinbo Hua

33. **Semiconductor Research Corporation, NSF/SRC Multi-core Program** (SRC 2009-TJ-1991), "Parameterized Architecture-Level Thermal Modeling and Characterization for Multi-Core Microprocessor Design", $120,000, Aug.1, 2009 to July 30, PI, Co-PI: Yinbo Hua

34. **National Science Foundation Supplemental REU** (NSF-0937305), $6000, June 2009 to June 2010. PI.

35. **National Science Foundation, Office of International Science and Engineering (OISE)**: Workshop Program, (OISE-0929699), "U.S.- ChinaWorkshop on Advanced Simulation and Design Techniques for Nanoscale VLSI Systems", $59,646, June 2009-May 2012, PI, co-PI: Albert Wang.

36. **UC MEXUS, 2009 UC MEXUS-CONACYT Collaborative Research Grant, "**Symbolic modeling and reduction for analog/RF circuits and on-chip interconnect", $25, 000, Aug 2009 to Jan 2011, PI, co-PI: Dr. Esteban Tlelo-Cuautle.

37. **Intel Corporation, "**Parameterized Thermal Behavioral Modeling and Simulation for Designing System Platforms", $50,000, PI, Nov., 2009 to Dec, 2010.

38. **National Science Foundation, NSF CCF Core Program** (CCF-1017090), "SHF:Small:GPU-Based Many-Core Parallel Simulation of Interconnect and High-Frequency Circuits", $270,000, Sept. 1, 2010 to Aug. 30, 2013. PI (single PI).

39. **National Science Foundation Supplemental REU** (NSF-1039796), $6000, June 2010 to June 2011. PI.

40. **University of California Academic Senate Research Fund**, $1050, July, 2010 to June 2011. PI.

41. **National Science Foundation Supplemental** (OISE-1051797), "US-Singapore Planning Visit: Collaborative Research on Design and Verification of 60Ghz RF/MM Integrated Circuits", $14,625,April 1, 2011 to March 31, 2012. PI.

42. **National Science Foundation Supplemental REU** (NSF-1128307), June 2011 to June 2012. $8000, PI.

43. **National Science Foundation, NSF CCF Core Program** (CCF-1116882), "SHF:Small:Variational and Bound Performance Analysis of Nanometer Mixed-Signal/Analog Circuits", Aug. 1, 2011 to July. 30, 2014. PI (single PI).

44. **University of California Academic Senate Research Fund**, July, 2010 to June 2011. PI.

45. **National Science Foundation, Office of International Science and Engineering (OISE):** (OISE-1130402), "IRES: Development of Global Scientists and Engineers by Collaborative Research on Variation-Aware Nanometer IC Design", $150K, Aug. 1, 2011 to July 30, 2014, PI.

46. **UC MEXUS, 2011 UC MEXUS-CONACYT Collaborative Research** Grant, "Symbolic and Statistical Modeling and Analysis Techniques for Analog/Mixed-Signal Nanometer Integrated Circuits", $25,000, Sept. 1 2011 to Feb. 30, 2013, PI, co-PI: Dr. Esteban Tlelo-Cuautle.

47. **Department of Education Graduate Assistance in Areas of National Need (GAANN) Fellowship** (P200A120099), "GAANN Fellowship in Electrical Engineering", $400K, Aug. 2012 to Aug. 2015, co-PI, PI: Yingbo Hua.

48. **National Science Foundation, NSF FRS (Failure Resistant Systems) program** (CCF-1255899), "Thermal-Sensitive System-Level Reliability Analysis and Management for Multi-Core and 3D Microprocessors", $180K, April 1, 2013 to March. 31, 2016. PI (single PI).

49. **Semiconductor Research Corporation, NSF/SRC Multi-core Program** (SRC 2013-TJ-2417), "Thermal-Sensitive System-Level Reliability Analysis and Management for Multi-Core and 3D Microprocessors", $120K, April 1st, 2013 to Match 30, 2016, PI.
50. **National Science Foundation Supplemental REU** (NSF-11063387), June 2013 to June 2014. $12,800, PI.
51. **Academic Senate COR (committee on research) Fellowships**, "Runtime Thermal Management for Multi/many Core and 3D Integrated Systems", $7500, July, 2013 to June 2014. PI.
52. **National Science Foundation CISE CCF Core Small program** (CCF-1527324), "SHF:Small: Physics-Based Electromigration Assessment and Validation For Reliability-Aware Design and Management", $450,000, June 1st, 2015 to May 31th 2018, single PI.
53. **National Science Foundation Supplemental REU** (CCF-1540083), June 2015 to June 2016. $12,800, PI.
54. **Defense Advanced Research Projects Agency (DARPA)** (HR0011-16-2-0009), "Advanced Modeling and Analysis for Accelerating Effects of Electromigration and Stress Migration for Copper Interconnects of ICs", $ 462,644, Feb. 2016-Aug, 2018 (30 months). Single PI.

Travel Grants, Student Grants, Donation (Gifts)

- Travel Grant, IEEE International Conference on Computer-Aided Design, 1997.
- Travel Grant, IEEE/ACM Design Automation Conference, 2001.
- Travel Grant, IEEE/ACM Design, Automation and Testing in Europe, (DATE), 2004.
- Travel Grant, IEEE Asia and South Pacific Design Automation Conferences (ASPDAC), 2006, ¥100,000 Japanese Yuan
- Altera Corporation , Quartus-II/Max-Plus II FPGA development software, July, 2002. $2000
- Altera Corporation, Altera UP2 development broad, July, 2002. $1100
- Altera Corporation , Excalibur Development Kit (Based on Nios Embedded Processor), , Sept. 2002. $4800
- Altera Corporation, Nios Development Kit (Stratix version), July, 2003. $5000
- Oscilloscopes and other signal process equipment, US Navy, Sept. 2004, $8860.
- National Science Foundation, NS—UCR MSRIP program, June 2005 – Sept. 2005 (for Amalia Aviles). PI. $3000.
- Undergraduate Senior Student Research Grant (for Winter/Spring 2006), Feb. 2006 (for Amalia Aviles) , $600.
- NSF East Asia and Pacific Summer Institutes for U.S. Graduate Students (EAPSI), (NSF 05-617, For Jeffery Fan), Summer 2006, $5000.
- Undergraduate Research, Scholarly Activity, and Creative Arts Grant, RFID Senior Design Project: RFIDOLOGY, $400, Spring 2007.
- Altera Corporation, ED2 (education and development) Board, Oct. 10, 2007, $500

- Altera Corporation, Quartus II License (3 long-term license), Oct. 10, 2007, $1500
- Undergraduate Research via Senior Design Program, FPGA based surveillance system, $400, Spring 2009.
- Nvidia Corporation, Quadro FX5800 and Tesla S1070 1U computing cards, July 10, 2009, $10,000
- Nvidia Corporation, two Tesla C2070 cards, five Quadra 2000 cards, book donations, TA matching fund, $14,200.
- Nvidia Corporation, CUDA Research Center Award: two Tesla C2075 cards, PGI OpenACC compiler license, 20 GeForce GTX 480 cards, $12,000, total $18K, April, 2012.
- Xilinx Corporation, DIGILAB-Atlys board and design software package, $1800, Oct. 2013 (via Taeyoung Kim's application)
- Nvidia Corporation, one Kelper K40 GPU card, $5400, Jan., 2014.
- Xilinx Corporation, EF-VIVADO-HLSFL and UEF-VIVADOSYSTEM-25, $13,074, Nov. 2014.
- Xilinx Corporation, DIGILABZedBoard-410-248PKIT, $790, Nov. 2014.
- Nvidia Corporation, the Titan X GPU card, $1000, March 2016.
- Nvidia Jetson TX1 development board (embedded visual computing) with built-in camera and 4K video encoder and decoder, $600, June 2016.

Graduate Students and Visiting Scholar Supervision

Ph.D. and M.S. student supervision

- **Dr. Junjie Yang** (Ph.D. UCR, graduated in 2005): Dissertation: "*Behavioral Modeling and Simulation of Analog Circuits*", Now Sr. R&D Engineer, Cadence Design Systems, San Jose, CA.
- **Mr. Weikun Guo**, (M.S., graduated in 2004), Thesis: "*Efficient transient simulation of on-chip power grid networks*", A high-tech company in San Jose, CA.

- **Dr. Hang Li**, (Ph.D, UCR, graduated in 2007), Dissertation title: "*Power and Thermal Integrity Analysis and Optimization for Nanometer VLSI Systems*" . First job: R&D Engineer, MICRO Technology, San Jose, CA.

- **Dr. Jeffrey Fan**, (Ph.D, UCR, graduated in 2007), Dissertation title: Process variation aware interconnect simulation and optimization in VLSI Design. First job: Assistant Professor, Florida International University, FL.

- **Dr. Wei Wu**, (Ph.D., graduated in 2008), co-supervised with Prof. Jun Yang, Dissertation title: "Power/Thermal Modeling and Dynamic Thermal Management for SRAM Structure" , First Job: Research Scientist, Intel Corporation, Santa Clara, CA.

- **Dr. Pu Liu**, (Ph.D, graduated in 2008), Dissertation title: "*Advanced Model Reduction and Simulation Techniques for Integrated Electronic and Thermal Circuits*", First job: Sr. R&D Engineer, Cadence Design System, San Jose, CA.

- **Dr. Ning Mi**, (Ph.D. graduated in 2010), Dissertation title "Statistical analysis for on-chip power grid networks and interconnects considering process variations", First job: Sr. R &D Engineer, Cadence Design Systsm, San Jose, CA.

- **Dr. Boyan Yuan**, (Ph.D, graduated in 2010), Dissertation title "Advanced non-Krylov Subspace Model Order Reduction Techniques for Interconnect Circuits", First job: Post-Doc, Taxes A&M University.

- **Dr. Dou Li**, (Ph.D. graduated in 2010), Dissertation title "Modeling, Characterization and Simulation of On-Chip Power Delivery Networks and Temperature Profile on Multi-Core Microprocessors", first job: Sr. R & D Engineer, IC Compiler group, Synopsys, Mountain View, CA.

- **Mr. Thom Eguia,** (M.S. graduated in 2010), Dissertation title "Package-level Thermal Behavioral Modeling for Multi-Core Microprocessors", first job: R & D Engineer, West Digital Corporation, Lake Forest, CA.

- **Mr. Ryan Rakid,** (M.S, graduated in 2010), Dissertation title "Comparison of Recent Algorithms in Model Order Reduction of Interconnect Circuits".

- **Dr. Ruijing Shen** (Ph.D. 2011), Dissertation title "Statistical performance characterization and analysis of nano-scale VLSI Circuits". First job: Senior R &D Engineer, PrimeTime group, Synopsys, Mountain View, CA.

- **Dr. Hai Wang**, (Ph.D. graduated in 2012), Dissertation title "Compact Modeling and Analysis for Electronic and Thermal Effects of Nanometer Integrated and Packaged Systems", first job, Associate Professor, University of Electronic Science and Technology of China (UESTC), Chendu, China.

- **Mr. Santiago RODRIGUEZ CHAVEZ**, M.S. student, Department of Electronics, Institute National Astrophysics, Optical and Electrics, from Oct. 2011 to June 2012. (Co-Advisor)

- **Mr. Adolfo Adair PALMA RODRIGUEZ,** M.S. student, Department of Electronics, Institute National Astrophysics, Optical and Electrics, from Oct. 2011 to June 2012. (Co-Advisor). (Participated his defense in INAOE in Sept, 2012).

- **Dr. Xuexin Liu,** (Ph.D. graduated in May 11, 2013), Dissertation title "Parallel and Statistical Analysis and Modeling of Nanometer VLSI Systems", first job, Senior R & D Engineer, IC Compiler group, Synopsys, Mountain View, CA.

- **Dr. Zao Liu,** (Ph.D. graduated in May 2014), Dissertation title " System-level thermal modeling and management for multi-core and 3D microprocessors", first job, Sr. Engineer, Intel Corporation, Chandler, AZ.

- **Ms. Sahana Swarup**, (2010, Ph.D. to be expected 2015),

- **Ms. Xin Huang ,** (Ph.D., 2012, expected 2016)

- **Mr. Kai He,** (Ph.D., 2012, expected 2016)

- **Mr. Yue Zhao,** (Ph.D, 2011, expected 2017)

- **Mr. Taeyoung Kim**, (Ph.D., 2013, CSE, expected 2017)

- **Mr. Hengyang Zhao**, (Ph.D., joined in Sept, 2014)
- **Mr. Daniel Quach**, (Ph.D, joined in Sept, 2014).
- **Ms. Vallabhaneni Yasya Srilekha** (M.S., joined in Sept 2014).

Postdoctoral Fellow and visiting scholar supervision

- **Dr. Xiaolong Yuan**, Associate Professor, School of Electronic and Information Engineering, Beijing Jiaotong University, from June 2006 to March 2007.
- **Dr. Ling Jiang**, Professor, Department of Computer Sciences, Xi'an Institute of Post & Telecommunication, Feb. 2008 to Aug. 2008.
- **Dr. Esteban Tlelo-Cuautle**, Professor, Department of Electronics, Institute National Astrophysics, Optical and Electrics, Nov. 2009 to July 2010.
- **Dr. Rui Li,** Associate Professor, School of Automation, University of Electronic Science and Technology of China, from Sept. 2011 to Aug. 2012.
- **Dr. Zhigang Hao,** Ph.D. student, School of Microelectronics, Shanghai Jiaotong University, Jan. 2010 to June, 2011.
- **Kuangya Zhai, M.S. student,** Department of Computer Science and Technology, Tsinghua University, from April 15 to July 15, 2012.
- **Mr. Santiago RODRIGUEZ CHAVEZ**, M.S. student, Department of Electronics, Institute National Astrophysics, Optical and Electrics, from Oct. 2011 to June 2012.
- **Mr. Adolfo Adair PALMA RODRIGUEZ,** M.S. student, Department of Electronics, Institute National Astrophysics, Optical and Electrics, from Oct. 2011 to June 2012.
- **Dr. Puying Tang,** Associate Professor, School of Automation, University of Electronic Science and Technology of China, from Sept. 2012 to Aug. 2013.
- **Ms Lingling Tan,** Ph.D. student, Department of Electrical Engineering, Tianjian University from Sept. 2013 to Aug. 2014.
- **Dr. Haibao Chen, Ph.D. (Xi'an Jiaotong University), Post-Doctoral Fellow,** from Oct. 1, 2013 to Sept. 30, 2014.
- **Dr. Xiaoli Zhi**, Ph.D., Associate Professor, Shanghai University, Shanghai, China, from June 2014 to June 2015.
- **Dr. Xiaodong Xie**, Ph.D., Associate Professor, from Feb. 16, 2015 to Feb. 15, 2016.
- **Dr. Zhongdong Qi, Ph.D. (Tsinghua University), Post-Doctoral Fellow**, from Sept. 19, 2015 to Sept. 18, 2016.

Course Taught in UC Riverside

- EE133: Solid State Electronics, F02
- EE175A/B: W07, S07, W09, S09
- EE213: Computer-Aided Electronic Circuit Simulation, W03, W04, S05, S06, S07, S08, S09, F10, F12, F13
- EE260: Physical Design Automation for VLSI Systems, S03, S04
- EECS217: GPU Architecture and Parallel Programming, S11, W12, W13
- EE/CS120: Logic Design, F03, F04, S05, F05, S06, F06. F03, F04, S05, F05, S06, F06, F07, W08, S08. F09, F10, F12.
- EE/CS168: W12.
- EE290: Directed Study, W03, F05(3), W06(4), S06(4), F07(5), W08.
- EE297: Directed Research, W04, S04, F05(1), W06(1), S06(1), W07, S07, F07(3), W08, S08, F08, S09, W09(4), F09
- EE299: Research For Thesis or Dissertation: W03, S03, F03, W04, S04, F04, W05, S05, F05(1), F06(5), W07(5), S07(3), F07(3), W08, S08, F08, W09(5), S09
- EE298, F07(2),
- CS299, F07(1),
- CS298, F07(1).
- HNPG 97 (Honor Lower-Division) Research, S07, F07.