Publication List for MSLAB (1994-present)

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Books

B1. Zhanhai Qin, Sheldon X.-D. Tan and Chung-Kuan Cheng, *Symbolic Analysis and Reduction of VLSI Circuits*, Springer Publisher, 2005, ISBN: 0-387-23904-9; e-ISBN: 0-387-23905-7.

B2. Sheldon X.-D. Tan and Lei He, *Advanced Model Order Reduction Techniques for VLSI Designs*, Cambridge University Press, 2007, ISBN-13 978-0-521-86581-4, ISBN-10 0-521-86581.

B3. Ruijing Shen, Sheldon X.-D. Tan and Hao Yu, *Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs*, Springer Publisher, March 2012, ISBN-10: 1461407877.

B4. Esteban Tlelo-Cuautle, Sheldon X.-D. Tan (Editors), *VLSI Design*, InTech Open Access Publisher, January 2012, ISBN 978-953-307-884-7.

B5. Guoyong Shi, Sheldon X.-D. Tan, Esteban Tlelo-Cuautle, "*Advanced Symbolic Analysis for VLSI Systems -- Methods and Applications*", Springer Publisher, 2014, ISBN 978-1-4939-1103-5

Book Chapters:

B6. C.-J. Shi and X.-D. Tan, "Canonical Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams" Part III and pp.344-361 in *Computer-Aided Design of Analog Integrated Circuit and Systems,* R. A. Rutenbar, G. E. Gielen and

B. A. Antao (ed) , IEEE Press & Wiley-Interscience, 2002. ISBN 0-471-22782-X.

B7. Sheldon X.-D. Tan, Ruijing Shen, "Chip-Level Statistical Leakage Modeling and Analysis", Chapter in *Recent Advancements in Modeling of Semiconductor Processes, Circuits and Chip-Level Interactions*, Rasit Onur Topaloglu, and Peng Li (Editors), Bentham Publishing (www.ebook-engineering.org), eISBN: 978-1-60805-074-1, Sept, 2011. (online permanent address)

B8. Sheldon X.-D. Tan, Esteban Tlelo-Cuautle, "Recent development in symbolic analysis: an overview", Chapter in *Design of Analog Circuits through Symbolic Analysis*, M. Fakhfakh, E. Tlelo-Cuautle and F.V. Fernández (Editors.), Bentham Science Publishers Ltd (www.ebook-engineering.org), ISBN: 9078-1-60805-095-6, 2012.

B9. Sheldon X.-D. Tan, "Symbolic analysis by determinant decision diagrams and applications", Chapter in *Design of Analog Circuits through Symbolic Analysis*, M. Fakhfakh, E. Tlelo-Cuautle and F.V. Fernández (Editors.), Bentham Science Publishers Ltd (www.ebook-engineering.org), ISBN: 9078-1-60805-095-6, 2012.

B10. Esteban Tlelo-Cuautle, Carlos Sanchez-Lopez, Elyoenai Martinez-Romero, Sheldon X.-D. Tan, Peng Li, Francisco Fernandez and Mourad Fakhfakh, "Behavioral modeling of mixed-mode integrated circuits", Esteban Tlelo-Cuautle, Editor, Chapter in "*Advances in Analog Circuits*", INTECH (www.intechweb.org), ISBN 978-953-307-323-1, Feb., 2011.

B11. Xue-Xin Liu, Hao Yu, Hai Wang, Sheldon X.-D. Tan, "Analog mismatch analysis by stochastic nonlinear macromodeling", Chapter in "Analog Circuits: Applications, Design and Performances", E. Tlelo-Cuautle (Editor), NOVA Science Publishers Inc. ISBN: 978-1-61324-355-8. Sept., 2011

B12. Sheldon X.-D. Tan, Xue-Xin Liu and Eric Mlinar, and Esteban Tlelo-Cuautle, "Parallel symbolic analysis of large analog circuits on GPU platforms", Chapter 6 in "VLSI Design", Esteban Tlelo-Cuautle and Sheldon X.-D. Tan (Editors), INTECH (www.intechweb.org), ISBN 978-953-307-884-7, January, 2012.

B13. S. Rodriguez-Chavez, A.A. Palma-Rodriguez, E. Tlelo-Cuautle, and S. X.-D. Tan, "Graph-based symbolic and symbolic sensitivity analysis of analog integrated circuits", Chapter in "*Analog/RF and Mixed-Signal Circuit Systematic Design*", Mourad Fakhfakh, Esteban Tlelo-Cuautle, R. Castro-Lopez (editors), Springer, 2012. ISBN 978-3-642-36328-3.

B14. X.-X. Liu, S. X.-D. Tan, H. Wang, and H. Yu, "GPU-accelerated envelope-following method", Chapter 17 in "*Designing Scientific Applications on GPU*", Raphael Couturier (Editor), CRC Press /Taylor & Francis Group, Nov. 2013. ISBN 9781466571648

Ph.D. Thesis

D1. Sheldon X.-D. Tan, "Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams", University of Iowa, 1999.

Ph.D. Student Theses

D2. Junjie Yang, "Behavioral Modeling and Simulation of Analog Circuits", University of California at Riverside, Dec.23, 2004.

D3. Jeffrey Fan, "Process variation aware interconnect simulation and optimization in VLSI Design", University of California at Riverside, May 8, 2007.

D4. Hang Li, "Power and Thermal Integrity Analysis and Optimization for Nanometer VLSI System", University of California at Riverside, May 18, 2007.

D5. Wei Wu, "Power/Thermal Modeling and Dynamic Thermal Management for SRAM Structure", University of California at Riverside, Feb. 15, 2008.

D6. Pu Liu, "Advanced Model Reduction and Simulation Techniques for Integrated Electronic and Thermal Circuit", University of California at Riverside, March. 3, 2008.

D7. Boyuan Yan, "Advanced non-Krylov Subspace Model Order Reduction Techniques for Interconnect Circuits", University of California at Riverside, Nov. 25, 2009.

D8. Ning Mi, "Statistical Analysis for On-chip Power Grid Networks and Interconnects Considering Process Variation", University of California at Riverside, Dec. 7, 2009.

D9. Duo Li, "Modeling, Characterization and Simulation of On-Chip Power Delivery Networks and Temperature Profile on Multi-Core Microprocessors", University of California at Riverside, September 15, 2010.

D10. Ruijing Shen, "Statistical Performance Characterization and Analysis of Nano-Scale VLSI Circuits", University of California at Riverside, Dec. 8, 2011.

D11. Hai Wang, "Compact Modeling and Analysis for Electronic and Thermal Effects of Nanometer Integrated and Packaged Systems", University of California at Riverside, April 10, 2012.

D12. Zhigang Hao, "Computer-Aided Design Methods for Variational Analysis of Nanosale Mixed-Signal Integrated Circuits", co-advised with Prof. Guoyong Shi of SJTU. May, 2012 and he got Ph.D. from SJTU.

D13. Xuexin Liu, "Parallel and Statistical Analysis and Modeling of Nanometer VLSI Systems", University of California at Riverside, March 11, 2013.

D14. Zao Liu, "System-level thermal modeling and management for multi-core and 3D microprocessors", University of California at Riverside, May 9, 2014.

D15. Kai He, “Parallel CAD algorithms and hardware security for VLSI Systems”, University of California at Riverside, July 29, 2016.

D16. Xin Huang, “Physics-Based Electromigration and Time Dependent Dielectric Breakdown Modeling and Reliability Analysis for Nanometer VLSI Circuits”, University of California at Riverside, July 29, 2016.

Conference Presentations (informal publication).

I1. Xuexin Liu, Kuangya Zhai, Sheldon X.-D. Tan, “Fast thermal analysis of 3D Integrated Circuits and CPU-GPU Platforms”, GPU Technology Conference, San Jose, March, 2013. (By Xuexin Liu).

I2. S. Ahn, H. Y. Chiang, L. Suasnabar, S. X.-D. Tan, J. Zhou, “Practical high-speed network modeling and analysis”, Southern California Conference for Undergraduate Research (SCCUR), California State at Fullerton, Nov. 2014. https://apps.fullerton.edu/CSUFConferences/SCCUR/Submission/Status?submissionCode=83C6NhWC

Tutorials:

T1. Paul M. Harvey, Howard Chen, Chung-Kuan Cheng, Manjid Borah, Lei He, and Sheldon X.-D. Tan, "High Performance Interconnect and Packaging", full day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference*, January 24, 2006.

T2. Sheldon X.-D. Tan, J. Fan, "Inductance Extraction and Compact Modeling of Inductively Coupled Interconnects in the Presence of Process Variations", half-day tutorial, IEEE ASICON'07, Oct. 2007 (**invited**).

T3. Sheldon X.-D. Tan, "Advanced modeling and analysis techniques for nanometer interconnect and multi-core VLSI circuits", ASIC & System Lab, **Fudan University**, July 27 to Aug. 1, 2008. (Four presentations were given in the short course), Shanghai, China.

T4. Sheldon X.-D. Tan and Hai Wang, "Architecture level thermal modeling, prediction and management for multi-core and 3D microprocessors", a half day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference*, Singapore, Singapore, January 24, 2014.

T5. Valeriy Sukharev, Sheldon Tan, Marko Chew, "Full-chip Electromigration Assessment and System-level EM Reliability Management", embedded tutorial, *IEEE/ACM International Conference on Computer-Aided Design* (ICCAD), San Jose, CA, Nov. 2014.

Patents:

P1. Sheldon X.-D. Tan, X. Wang, B.A. Fairbanks, "I/O Pin Placement Algorithm For Programmable Logic Devices" Filed on May, 2003. U.S. Patent No. 7111265 (approved on 9/19/2006).

P2. Sheldon X.-D. Tan, B. Yan, "Decentralized complexity reduction of parasitic interconnect circuits", UC Case No. 2008-783-1, US provisional patent. (filed on May 28, 2008)

P3. Sheldon X.-D. Tan, D. Li, "Extended truncated balanced realization method for on-chip power grid network analysis", UC Case No. 2008-784-1, US provisional patent. (filed on Feb. 27, 2008).

P4. X. Hong, Y, Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, "Transient analysis of on-chip power grid networks based on equivalent circuits", Patent No. ZL 03104770.X (China)

P5. X. Hong, Y, Cai, J. Fu, Y. Luo, Z. Pan, Sheldon X.-D. Tan, "Fast decap allocation

method for noise reduction in the on-chip power grid networks", Patent No. ZL031570526 (China)

P6. X. Hong, Y, Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, "Relaxed hierarchical transient analysis method for power grid networks", Patent No. ZL 200510011804.2 (China)

Journal Articles

J1. X.-D. Tan, J.-R. Tong, and P.-S. Tang. "A general algorithm for multi-way digital circuit partitioning." *Chinese Journal of Electronics*, vol. 24, no. 8, 1996.

J2. X.-D. Tan, J.-R. Tong, and P.-S. Tang. "A multiple-optimization algorithm for multiple way VLSI network partitioning," *Chinese Journal of Computers* , vol. 19, no. 5, 1996.

J3. C.-J. Shi and X.-D. Tan. "Canonical symbolic analysis of large analog circuits with determinant decision diagrams." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 1-18, 2000.

J4. X.-D. Tan and C.-J. Shi. "Hierarchical symbolic analysis of analog integrated circuits via determinant decision diagrams." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 4, pp. 401-412, 2000.

J5. C.-J. Shi and X.-D. Tan. "Compact representation and efficient generation of s-expanded symbolic network functions for computer-aided analog circuit design." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 7, pp. 813-827, 2001.

J6. S. X.-D. Tan and C.-J. Shi. "Efficient vary large scale integration power/ground network sizing based on equivalent circuit modeling." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 3, pp.277-284, 2003.

J7. X.-D. Tan and C.-J. Shi. "Balanced multi-level multi-way partitioning of large analog integrated circuits for hierarchical symbolic analysis." *Integration, The VLSI Journal,* vol 34/1-2 pp 65 – 86, 2003.

J8. X.-D. Tan, C.-J. Shi and F. J.-C. Lee. "Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings.", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. vol. 22, no. 12, pp. 1678-1684, Dec. 2003.

J9. S. X.-D. Tan and C-J. Shi. "Efficient DDD-based interpretable symbolic characterization of large analog circuits", *IEICE Transactions on Fundamentals*, pp.3112-3118, vol. E86-A, No.12, Dec. 2003.

J10. S. X.-D. Tan and C-J. Shi, "Efficient approximation of symbolic expressions for analog behavioral modeling and analysis." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 23, No.6, pp. 907-918, June 2004.

J11. W. Guo, S. X.-D. Tan, Z. Luo, X. Hong, "Partial random walks for transient analysis of large power distribution networks", *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Science*, vol. E87-A, No. 12 pp. 3265-3272, December 2004.

J12. J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan and Z. Pan, "A fast decoupling capacitor budgeting algorithm for robust on-chip power delivery", *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Science*, vol. E87-A, No. 12 pp.3273-3280, December 2004.

J13. S. X.-D. Tan, "A general hierarchical circuit modeling and simulation algorithm", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 3, pp. 418-434, March 2005.

J14. X.-D. S. Tan, W. Guo and Z. Qi, "Hierarchical approach to exact symbolic analysis of large analog circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 8, pp. 1241-1250, 2005.

J15. Y. Zou, Y. Cai, Q. Zhou, X. Hong, S. X.-D. Tan, "A fast delay computation for the hybrid structured clock network", *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Science*, Vol.E88-A No.7 pp.1964-1970, July 2005.

J16. Z. Qi,, H. Yu, P. Liu, S. X.-D. Tan, L. He, "Wideband passive multi-port model order reduction and realization of RLCM circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* (TCAD), vol. 25, No. 8, pp. 1496-1509, Aug. 2006.

J17. J. Yang, S. X.-D. Tan, "Nonlinear transient and distortion analysis via frequency-domain Volterra series", *Journal of Circuits, Systems and Signal Process*, vol. 25, No. 3, pp.295-314, 2006.

J18. H. Li, J. Fan, Z. Qi, S. X.-D. Tan, L. Wu, Y. Cai, X. Hong, "Partitioning-based approach to fast on-chip decoupling capacitance budgeting and minimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 25, no. 11, pp.2402-2412, Nov. 2006.

J19. P. Liu, H. Li, L. Jin, W. Wu, S. X.-D. Tan and J. Yang, "Fast thermal simulation for runtime temperature tracking and management", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System,* vol. 25, no. 12, pp. 2882-2893, 2006.

J20. Y. Cai, J. Fu, X. Hong, S. X.-D. Tan, Y. Luo, "Power/ground network optimization considering decap leakage currents", *IEEE Transaction on Circuit and System II,* vol. 53, no. 10, pp.1012-1016, Oct. 2006.

J21. S. X.-D. Tan, "Symbolic analysis of analog circuits by Boolean logic operations", *IEEE Trans. Circuit and Systems-II*, vol. 53, no. 11, pp.1313-1317, Nov. 2006.

J22. J. Fan, S. X.-D. Tan, Y. Cai and X. Hong, "Partitioning-based decap capacitor budgeting via sequence of linear programming", *Integration, The VLSI Journal,* vol. 40, no.4, pp. 516-524, 2007.

J23. P. Liu, S. X.-D. Tan, J. Kong, B. McGaughy, L. He, "TermMerg: An efficient terminal reduction method for interconnect circuits" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 26, no. 8, pp1382-1392, 2007.

J24. Y. Cai, Z. Pan, S. X.-D. Tan, X. Hong, J. Fu, "Fast analysis of power/ground networks via circuit reduction", Chinese Journal of Semiconductors, vol. 26, no. 7, pp.1340-1345, 2005.

J25. J. Shi, Y. Cai, J. Fan, S. X.-D. Tan and X. Hong, "Pattern based iterative method for extreme large power/ground analysis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 26, no. 4, pp.680-692, April 2007.

J26. W. Wu, L. Jin, , J. Yang, P. Liu and S. X.-D. Tan, "Efficient power modeling and software thermal sensing for runtime temperature monitoring ", *ACM Transaction on Design Automation of Electronic Systems* (TODAES), vol. 12, no. 3, August, 2007.

J27. B. Liu, S. X.-D. Tan, "Minimum decoupling capacitor insertion in VLSI power/ground supply networks by semidefinite and linear programs", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 15, no. 11, pp. 1284-1287, Nov. 2007

J28. Z. Luo, Y. Cai, S. X.-D. Tan, X. Hong, Y. Wang, Z. Pan, J. Fu, "Time-domain analysis methodology for large-scale RLC circuits and its applications", *Science in China F Series*, vol. 49, no. 5, pp. 665-680, Oct., 2006.

J29. P. Liu, S. X.-D. Tan, B. Yan, B. McGaughy, "An efficient terminal and model order reduction algorithm", *Integration, the VLSI Journal*, vol.41, no.2, pp.210-218, Feb. 2008. (online permanent DOI link)

J30. Y. Cai, L. Kang, J. Shi and X. Hong and S. X.-D. Tan, "Random walk guided decap embedding for power/ground network optimization", *IEEE Trans. Circuit and Systems-II* (TCAS-II), vol. 55, no. 1, pp.36-40, Jan. 2008.

J31. Y. Cai, J. Shi, Z. Pan, X. Hong and S. X.-D. Tan, "Large scale P/G grid transient simulation using hierarchical relaxed approach", *Integration, the VLSI Journal*, vol.41, no.1, pp.153-160, Jan. 2008.

J32. N. Mi, J. Fan, S. X.-D. Tan, Y. Cai and X. Hong, "Statistical analysis of on-chip power delivery networks considering lognormal leakage current variations with spatial correlations", *IEEE Transaction on Circuit and System I* (TCAS-I), vol. 55, no. 7, pp.2064-2075, August, 2008.

J33. B. Yan, S. X.-D. Tan, B. McGaughy, "Second-order balanced truncation for passive-order reduction of RLCK circuits", *IEEE Transaction on Circuit and System II* (TCAS-II), vol. 55 no. 9, pp. 942-946, Sept 2008.

J34. N. Mi, B. Yan, S. X.-D. Tan, "Multiple block structure-preserving reduced order modeling of interconnect circuits" *Integration, The VLSI Journal*. vol. 42, no. 2, pp.158-168, 2009, (online permanent DOI link)

J35. S. X.-D. Tan, P. Liu, L. Jiang, W. Wu, M. Tirumala, "A fast architecture-level

thermal analysis method for runtime thermal regulation", *ASP Journal of Low Power Electronics* (JOLPE), vol. 4, no. 4, August, pp.139-148, 2008.

J36. N. Mi, S. X.-D. Tan, Y. Cai and X. Hong, "Fast variational analysis of on-chip power grids by stochastic extended Krylov subspace method", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), vol. 27, no. 11, pp. 1996-2006, 2008.

J37. D. Li, S. X.-D. Tan, L. Wu, "Hierarchical Krylov subspace based reduction of large interconnects", *Integration*, *The VLSI Journal*, vol. 42, no.2, pp193-202, 2009. (online permanent DOI link)

J38. D. Li, S. X.-D. Tan, E. H. Pacheco, M. Tirumala, "Architecture-level thermal characterization for multi-core microprocessors", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 17, no. 10, pp. 1495-1507, October, 2009.

J39. R. Shen, S. X.-D. Tan, J. Cui, W. Yu, Y. Cai and G. Chen, "Variational capacitance extraction and modeling based on orthogonal polynomial method", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol.18, no.11, pp1556-1565, 2010.

J40. H. Yu, C. Chu, Y. Shi, D. Smart, L. He and S. X.-D. Tan, "Fast analysis of a large-scale inductive interconnect by block-structure-preserved macromodeling", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 18, no. 10, pp.1399-1411, 2010.

J41. D. Li, S. X.-D. Tan, "Fast analysis of on-chip power grid circuits by extended truncated balanced realization method", *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Science*, vol. E92-A, no. 12, pp.3061-3069, 2009.

J42. R. Shen, S. X.-D. Tan, N. Mi and Y. Cai, "Statistical modeling and analysis of chip-level leakage power by spectral stochastic method", *Integration*, *The VLSI Journal*, vol. 43, no. 1, pp. 156-165, January 2010. (online permanent DOI Link)

J43. D. Li, S. X.-D. Tan, E. H. Pacheco, M. Tirumala, "Parameterized architecture-level thermal modeling for multi-core microprocessors", *ACM Transaction on Design Automation of Electronic Systems* (TODAES), vol. 15, no. 2, pp.1-22, February 2010 (**one of top 10 downloaded ACM TODAES Articles published in 2010**).

J44. S. X.-D. Tan, B. Yan and H. Wang, "Recent advance in non-Krylov subspace model order reduction of interconnect circuits*", Tsinghua Science and Technology*, vol.15, no. 2, pp.151-168, April, 2010. (**invited**) (online permanent link)

J45. D. Li, S. X.-D. Tan, "Statistical analysis of large on-chip power grid networks by variational reduction scheme", *Integration*, *The VLSI Journal*, vol. 43, no. 2, pp.167-175, April, 2010.

J46. E. Tlelo-Cuautle, C. Sanchez-Lopez, E. Martınez-Romero, S. X.-D. Tan, "Symbolic analysis of analog circuits containing voltage mirrors and current mirrors", *Analog Integr Circ Sig Process*, vol. 65, no. 1, pp. 89-95, 2010, (online

permanent DOI Link)

J47. B. Yan, S. X.-D. Tan and J. Fan, "Passive rational interpolation based reduction via Caratheodory extension for general systems", *IEEE Transaction on Circuit and System II* (TCAS-II), vol. 57, no. 9, pp. 750-755, Sept, 2010.

J48. T. Eguia, S. X.-D. Tan, R. Shen, D. Li, E. H. Pacheco, M. Tirumala, L. Wang, "General parameterized thermal modeling for high-performance microprocessor design", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), Vol. 20, No. 2, pp.221-224, Feb. 2012. 10.1109/TVLSI.2010.2098054.

J49. C. Sánchez-López, F.V. Fernández, E. Tlelo-Cuautle, S. X.-D. Tan, "Pathological element-based active device models and their application to symbolic analysis," *IEEE Transactions on Circuits and Systems I* (TCAS-I) , vol. 58, no 6, pp.1382-1395, 2011.

J50. B. Yan, S. X.-D. Tan, L. Zhou, J. Chen, R. Shen, "Decentralized and passive model order reduction of linear networks with massive ports", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), pp.865-876, vol. 20, no. 5, May 2012, 10.1109/TVLSI.2011.2126612.

J51. H. Wang, H. Yu, S. X.-D. Tan, "Fast timing analysis of clock networks considering environmental uncertainty", *Integration*, *The VLSI Journal*, vol. 45, no. 4, pp.376-387, Sept 2012. online available at http://dx.doi.org/10.1016/j.vlsi.2011.03.001

J52. Z. Hao, S. X.-D. Tan, E. Tlelo-Cuautle, J. Relles, C. Hu, W. Yu, Y. Cai and G. Shi, "Statistical extraction and modeling of inductance considering spatial correlation", *Analog Integr Circ Sig Process*, July 2011. DOI: 10.1007/s10470-011-9720-8.

J53. H. Wang, S.X.-D. Tan, R. Rakid, "Compact modeling of interconnect circuits over wide frequency band by adaptive complex-valued sampling method", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 17, no. 1, pp.5:1-5:22, January 2012. 10.1145/2071356.2071361

J54. F. Gong, X. Liu, H. Yu, S. X.-D. Tan, J. Ren and L. He, "A fast non-Monte-Carlo yield analysis and optimization by stochastic orthogonal polynomials", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 17, no.1, pp10:1-10:23, January 2012. 10.1145/2071356.2071366

J55. Z. Hao, S. X.-D. Tan, G. Shi, "Statistical full-chip total power estimation considering spatially correlated process variations", *Integration*, *The VLSI Journal*, Vol. 73, no. 1, 2012. doi:10.1016/j.vlsi.2011.12.004

J56. Z. Luo, G. Zhao, J. A. Gordon, S. X.-D. Tan, "Localized relaxation theory of circuits and its application in electro-thermal analysis", *Science China Information Sciences*, Jan. 2012 (DOI: 10.1007/s11432-011-4479-1).

J57. R. Shen, S. X.-D. Tan, H. Wang, J. Xiong, "Fast statistical full-chip leakage analysis for nanometer VLSI systems", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 17, no. 4, pp.51:1--51:19, Sept. 2012. 10.1145/2348839.2348855

J58. Z. Hao, G. Shi, S. X.-D. Tan, E. Tlelo-Cuautle, "Symbolic moment computation

for statistical analysis of large interconnect networks", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 21, no. 5, pp. 944-957, May 2013

J59. H. Wang, S. X.-D. Tan, D. Li, A. Gupta, Y. Yuan, "Composable thermal modeling and simulation for architecture-level thermal designs of multi-core Microprocessors", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 18, no. 2, March 2013.

J60. X. Liu, S. X.-D. Tan, A. Palma-Rodriguez, E. Tlelo-Cuautle, G. Shi, and Y. Cai, "Performance bound analysis of analog circuits in frequency and time domain considering process variations", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 19, no. 6, Dec. 2013.

J61. Z. Liu, S. X.-D. Tan, H. Wang, Y. Hua, and A. Gupta, "Compact thermal modeling for packaged microprocessor design with practical power maps", *Integration*, *The VLSI Journal*, vol. 47, no. 1, January 2014. (**One of the most downloaded papers in 2014 after its publication, 178 downloads in 3 months**) see: http://www.journals.elsevier.com/integration-the-vlsi-journal/most-downloaded-articles/ Online access: http://www.sciencedirect.com/science/article/pii/S0167926013000412

J62. Z. Liu, S. Swarup, S. X.-D. Tan, H. Chen, H. Wang, "Compact lateral thermal resistance model of TSVs for fast finite-difference based thermal analysis of 3D stacked ICs", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), vol. 33, no. 10. Oct. 2014.

J63. X. Liu, S. X.-D. Tan, H. Yu, "A GPU-accelerated parallel shooting algorithm for analysis of radio frequency and microwave integrated circuits", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 23, no. 3, March 2015. http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6777551

J64. Z. Liu, S. X.-D. Tan, X. Huang and H. Wang, "Task migrations for distributed thermal management considering transient effects", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 23, no. 2, Feb. 2015.

J65. X. Liu, K. Zhai, Z. Liu, K. He, S. X.-D. Tan, and W. Yu, "Parallel thermal analysis of 3D integrated circuits with liquid cooling on CPU-GPU platforms", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 23, no. 3, pp. 575-579, March 2015.

J66. H. Chen, S. X.-D. Tan, D. H. Shin, X. Huang, H. Wang and G. Shi, "H^2-Matrix-based Finite Element Linear Solver for Fast Transient Thermal Analysis of High-Performance ICs", *Int. J. Circ. Theor. Appl.*, vol. 43, no.2, Nov. 2014, DOI: 10.1002/cta.2051.

J67. H. Chen, Y. Li, S. X.-D. Tan, X. Huang, H. Wang and N. Wong, "*H*-matrix based finite-element-based thermal analysis for 3D ICs", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol. 20, no. 47, pp. 47:1-25, 2015.

J68. K. He, S. X.-D. Tan, H. Wang and G. Shi, "GPU-accelerated parallel sparse LU factorization method for fast circuit analysis", *IEEE Transactions on Very Large Scale Integrated Systems* (TVLSI), vol. 24, no.3, pp.1140-1150, March 2016.

J69. V. Sukharev, X. Huang and S. X.-D. Tan, "Electromigration induced stress evolution under alternate current and pulse current loads", *Journal of Applied Physics*, 118, 034504, 2015, published on line: http://scitation.aip.org/content/aip/journal/jap/118/3/10.1063/1.4926794 , DOI: 10.1063/1.4926794.

J70. K. He, S. X.-D. Tan, H. Zhao, X. Liu, H. Wang and G. Shi, "Parallel GMRES solver for fast analysis of large linear dynamic systems on GPU platforms", *Integration*, *The VLSI Journal*, Vol. 52, Jan. 2016, pp. 10-22, doi:10.1016/j.vlsi.2015.07.005 http://dx.doi.org/10.1016/j.vlsi.2015.07.005

J71. Y. Zhao, T. Kim, H. Shin, S. X.-D. Tan, X. Li, H. Chen and H. Wang "Statistical rare event analysis and parameter guidance by elite learning sample selection", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), Vol. 21, No.4. pp.56:1-56:21, May 2016.

J72. H. Wang, J. Ma, S. X.-D. Tan, C. Zhang, H. Tang, and K. Huang, "Hierarchical dynamic thermal management method for high-performance many-core microprocessors", *ACM Transactions on Design Automation of Electronic Systems* (TODAES), Vol 22, No.1, 1:1-1:21, July 2016.

J73. K. He, X. Huang, S. X.-D. Tan, "EM-based on-chip aging sensor for detection of recycled ICs", *IEEE Design & Test*, pp.56-64, June, 2016.

J74. X. Huang, A. Kteyan, S. X.-D. Tan, V. Sukharev, "Physics-based electromigration models and full-chip assessment for power grid networks", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), Vol. 35, No. 11, pp.1848-1861, Nov. 2016.

J75. H. Chen, S. X.-D. Tan, X. Huang, T. Kim, V. Sukharev, "Analytical modeling and characterization of electromigration effects for multi-branch interconnect trees", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), Vol. 35, No. 11, pp.1811-1824, Nov. 2016.

J76. X. Huang, V. Sukharev, J.-H. Choy, M. Chew, T. Kim, S. X.-D. Tan, "Electromigration assessment for power grid networks considering temperature and thermal stress effects", *Integration*, *The VLSI Journal*, (in press) http://dx.doi.org/10.1016/j.vlsi.2016.04.001

J77. X. Huang, V. Sukharev, T. Kim and S. X.-D. Tan, "Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing", *Integration, The VLSI Journal* 2016 (in press).

Symposia/Conference Proceedings

C1 X.-D. Tan, J.-R. Tong, P.-S. Tang, "Design tool integration and control using object oriented approach," *Proc. Int. Application Specific Integrated Circuits Conference* (ASICON'94), Beijing P.R. China, Oct. 1994, pp.21-24.

C2 X.-D. Tan, J.-R. Tong., P.-S. Tang, "Improved min-cut algorithm for multi-way VLSI network partitioning," *Proc. Int. Computer Aided Design and Graphics* (CAD/Graphic'95), Wuhan P.R. China, Oct. 1995, pp. 651-656.

C3 X.-D. Tan, J.-R. Tong, and P.-S. Tang, "An efficient multi-way algorithm for balanced partitioning of VLSI circuits," *Proc. IEEE Int. Conf. on Computer Design* (ICCD), Austin, TX, Oct. 1997, pp. 608-613.

C4 C.-J. Shi, Y. Ye, and X.-D Tan, "Behavioral model optimization via sensitivity-enhanced genetic search," *Proc. IEEE/VIUF Int. Workshops on Behavioral Modeling and Simulation* (BMAS'97), Washington DC, Oct. 1997, pp. 17-24.

C5 C.-J. Shi and X.-D. Tan, "Symbolic analysis of large analog circuits by determinant decision diagrams," *Proc. IEEE International Conference on Computer-Aided Design* (ICCAD'97), San Jose, CA. Nov. 1997, pp. 366-373.

C6 C.-J. Shi and X.-D. Tan, "Efficient derivation of exact s-expanded symbolic expressions for behavioral modeling of analog circuits," *Proc. IEEE Custom Integrated Circuits Conference* (CICC98), Santa Clara, CA, May, 1998, pp. 463-466.

C7 X.-D. Tan and C.-J Shi, "Hierarchical symbolic analysis of large analog circuits with determinant decision diagrams," *Proc. IEEE International Symposium on Circuits and Systems* (ISCAS), vol. VI, Monterey, CA. May 31-June 3, 1998, pp. 318-321.

C8 X.-D. Tan and C.-J. Shi, "Balanced multi-level multi-way partitioning of large analog circuits for hierarchical symbolic analysis," *Proc. Asia and South Pacific Design Automation Conference* (ASP-DAC'99), Hong Kong, China. Jan. 18-21, 1999, pp.1-4.

C9 X.-D. Tan and C.-J. Shi, "Interpretable symbolic small-signal characterization of large analog circuits using determinant decision diagrams," *Proc. Design, Automation and Test in Europe* (DATE'99), Munich, Germany, Mar. 10-13, 1999, pp. 448-453

C10 X.-D. Tan, C.-J. Shi, D. Lungeanu, J.-C. Lee, and L.-P. Yuan, " Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings," *Proc. IEEE/ACM 36th Design Automation Conference* (DAC), New Orleans, LA. June 1999, pp. 78-83. **Best Paper Award (< 1%)**

C11 X.-D. Tan and C.-J. Shi., "Symbolic circuit-noise analysis and modeling via determinant decision diagrams," *Proc. Asia and South Pacific Design Automation Conference* (ASP-DAC'00), Yokohama, Japan. Jan. 2000, pp. 283-287.

C12 X.-D. Tan and C.-J. Shi, "Fast power ground network optimization based on equivalent circuit modeling," *Proc. 38th IEEE/ACM Design Automation Conference* (DAC'2001), Las Vegas, NE. June 2001, pp.550-554.

C13 X.-D. S. Tan, C.-J. Richard Shi, "Parametric analog behavioral modeling based on cancellation-free DDDs", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS'02), Santa Rosa, CA, Oct., 2002.

C14 S. X.-D. Tan, C.-J. Shi, "Efficient DDD-based term generation algorithm for analog circuit behavioral modeling," *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'03), Kitakyushu, Japan, Jan. 2003, pp.789-794.

C15 Qi-De Qian and S. X.-D. Tan, "Advanced physical models for mask data verification and impacts on physical layout synthesis." *Proc. International symposium on quality electronic design* (ISQED'03), San Jose, March 2003, pp.125-130.

C16 S. X.-D. Tan and J. Yang, "Hurwitz stable model reduction for non-tree structured RLCK circuits," in Proc. *16th IEEE International System-on-Chip Conference* (SOC'03), Portland OR, Sept. 2003. pp.239-242.

C17 W. Guo and S. X.-D. Tan, "Circuit level alternating-direction-implicit approach to transient analysis of power distribution networks", in Proc. 5th *International Conference on ASIC* (ASICON'03), Beijing, China, Oct. 2003. pp.246-249, (**Invited**)

C18 S. X.-D. Tan, "A general s-domain hierarchical network reduction algorithm", Proc. *IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), San Jose, CA, pp. 650-657, Nov. 2003.

C19 J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan and Z. Pan "A fast decoupling capacitor budgeting algorithm for robust on-chip power delivery", *Proc. Asia South Pacific Design Automation Conference (ASP-DAC'04)*, pp.505-510, Yokohama, Japan, Jan. 2004.

C20 S. X.-D. Tan and Z. Qi and H. Li, "Hierarchical modeling and simulation of large analog circuits", *Proc. Design, Automation and Test in Europe* (DATE'04), Paris, France. pp. 740-741, Feb. 16-20, 2004.

C21 Z. Pan, Y. Cai, S. X.-D. Tan, Z. Luo, X. Hong ,"Transient analysis of on-chip power distribution networks using equivalent circuit modeling", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'04), pp. 63-68, San Jose, CA , March 2004.

C22 J. Yang and S. X.-D. Tan, "Behavioral modeling of analog circuits by dynamic semi-symbolic analysis", *Proc. IEEE International Symposium on Circuits and Systems* (ISCAS), Vancouver, pp. V105-108, May, 2004.

C23 J. Yang and S. X.-D. Tan, "An efficient algorithm for transient and distortion analysis of mildly nonlinear analog circuits", *Proc. IEEE International Symposium on Circuits and Systems* (ISCAS), Vancouver, Canada, pp. V129-132, May, 2004.

C24 W. Guo, S. X.-D. Tan, Z. Luo, X. Hong, "Partial random walk for large linear network analysis", *Proc. IEEE International Symposium on Circuits and Systems*

(ISCAS), Vancouver, Canada, pp. V173-176, May, 2004.

C25 S. X.-D. Tan and W. Guo and Z. Qi, "Hierarchical approach to exact symbolic analysis of large analog circuits", *Proc. 41th IEEE/ACM Design Automation Conference* (DAC'2004), pp.860-863, San Diego , CA, 2004.

C26 R. Lysecky, F. Vahid, S. X.-D. Tan, "Dynamic FPGA routing for just-in-time FPGA compilation", *Proc. 41th IEEE/ACM Design Automation Conference* (DAC'2004), San Diego , pp. 954-959, CA, 2004.

C27 H. Yu, L. He and S. X.-D. Tan, "Compact macro-modeling for on-chip RF passive components", *Proc. IEEE International Conference on Communications, Circuits and Systems,* Chengdu, vol. 2, pp. 199-202, China, 2004 .

C28 J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan and Z. Pan, "Simultaneous wire sizing and decoupling capacitance budgeting for robust on-chip power delivery", *Intl. Workshop Power and Timing Modeling, Optimization and Simulation*, (PATMOS'04), pp. 433-441, Greek.

C29 L. Zhang, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan, J. Fu, "Optimal wire sizing in the early stage design of on-chip power/ground (P/G) networks", *Int, Conf. Solid State and Integrated Circuit Technology* (ICSICT'04), Beijing, China, vol.3, pp.1936-1939, Oct. 2004.

C30 X. Wang, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan, "EQUADI: A linear complexity algorithm for transient analysis for power/ground(P/G) networks in ASICs", *Int, Conf. Solid State and Integrated Circuit Technology* (ICSICT'04), Beijing, China, vol. 3, pp.1952-1955, Oct. 2004.

C31 Y. Zou, Y. Cai ,Q. Zhou, X. Hong, S. X.-D. Tan, "A fast delay analysis algorithm for the hybrid structured clock network", in *Proc. Int. Conf. Computer Design* (ICCD), pp.344-349, 2004

C32 Z. Qi , S. X.-D. Tan, H. Yu , L. He and P. Liu, "Wideband modeling of RF/analog circuits via hierarchical multi-point model order reduction", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'05), pp.224-229. Shanghai, China, Jan. 2005.

C33 H. Yu, Z. Qi, L. He and S. X.-D. Tan, "A wideband hierarchical circuit reduction for massively coupled interconnects", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'05), pp.111-114, Shanghai, China, Jan. 2005.

C34 J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan and Z. Pan, "VLSI on-chip power / ground network optimization considering decap leakage currents", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'05), pp.735-738, Shanghai, China, Jan. 2005.

C35 Z. Pan, Y. Cai, Z. Luo, X. Hong, S. X.-D. Tan, W. Hou, L. Wu, "Relaxed hierarchical power/ground grid analysis", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'05), pp.1090-1093, Shanghai, China, Jan. 2005.

C36 Y. Zou, Q. Zhou, Y. Cai, X. Hong and S. X.-D. Tan, "Analysis of buffered hybrid structured clock networks", *Proc. Asia South Pacific Design Automation*

Conference (ASP-DAC'05), pp.93-98, Shanghai, China, Jan. 2005.

C37 P. Liu, Z. Qi and S. X.-D. Tan, "Passive hierarchical model order reduction and realization of RLCM circuits", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'05), pp. 603-608, San Jose, CA, March 2005.

C38 Z. Qi, and H. Li, S. X.-D. Tan, L. Wu, Y. Cai, X. Hong ,"Fast decap allocation algorithm for robust on-chip power delivery", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'05), pp. 542-547, San Jose, CA, March 2005.

C39 R. Lysecky, F. Vahid, S. X.-D. Tan, "A study of the scalability of on-chip routing for just-in-time FPGA compilation", *Proc. IEEE Symposium on Field-Programmable Custom Computing Machines*(FCCM'05), Napa, CA, April 2005.

C40 H. Li, Z. Qi, S. X.-D. Tan, L. Wu, Y. Cai, X. Hong, "Partitioning-based approach to fast on-chip decap budgeting and minimization", *Proc. IEEE/ACM Design Automation Conference* (DAC'2005), pp. 170-175, CA, 2005. **Best Paper Award Nomination (16 out of 735 submission, 2%)**

C41 J. Shi, Y. Cai, X. Hong, S. X.-D. Tan, "Efficient simulation of power/ground networks with packages and vias", *Intl. Workshop Power and Timing Modeling, Optimization and Simulation* (PATMOS'05), pp.257-266, Leuven, Belgium, Sep. 2005.

C42 P. Liu, Z. Qi, A. Aviles, S. X.-D. Tan, "A general method for multi-port active network reduction and realization", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.7-12, San Jose, CA, Sept., 2005.

C43 Z. Qi, S. X.-D. Tan, P. Liu, "Efficient analog circuit modeling by Boolean logic operations", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp. 76-81, San Jose, CA, Sept., 2005.

C44 J. Yang, S. X.-D. Tan, Z. Qi, M. Gawecki, "Hierarchical symbolic piecewise-linear circuit analysis", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.140-145, San Jose, CA, Sept., 2005.

C45 H. Yu, L. He, S. X.-D. Tan, "Block structure preserving model reduction", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.1-6, San Jose, CA, Sept., 2005.

C46 H. Li, P. Liu, Z. Qi, L. Jin, W. Wu, S. X.-D. Tan, and J. Yang, "Efficient thermal simulation for run-time temperature tracking and management", in *Proc. Int. Conf. Computer Design* (ICCD), pp.130-133, San Jose, CA 2005.

C47 Z. Qi, J. Fan, H. Li, S. X.-D. Tan, Y. Cai, X. Hong, "On-chip decoupling capacitor budgeting by sequence of linear programming", in Proc. *6th International Conference on ASIC* (ASICON), pp.98-101, Beijing China, Oct. 2005. (**Invited**).

C48 P. Liu, S. X.-D. Tan, H. Li, Z. Qi, J. Kong, B. McGaughy, L. He, "An efficient method for terminal reduction of interconnect circuits considering delay variations", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp. 821-826, San Jose, CA, Nov. 2005.

C49 P. Liu, Z. Qi, H. Li, L. Jin, W. Wu, S. X.-D. Tan and J. Yang, "Fast thermal

simulation for architecture level dynamic thermal management", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp.639-644, San Jose, CA, Nov. 2005.

C50 J. Shi, Y. Cai, S. X.-D. Tan, X. Hong, " Efficient early stage resonance estimation techniques for C4 package", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'06), pp.826-831, Yokohama City, Japan, Jan. 2006.

C51 J. Fan, I. Liao, S. X.-D. Tan, Y. Cai, X. Hong, "Localized on-chip power delivery network optimization via sequence of linear programming", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'06), pp.272-277, San Jose, CA, March 2006.

C52 P. Liu, S. X.-D. Tan, B. McGaughy, L. Wu, "Compact reduced order modeling for multiple-port interconnects", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'06), pp.413-418, San Jose, CA, March 2006.

C53 A. Kahng, B. Liu, S. X.-D. Tan, "SMM: Scalable analysis of power delivery networks by stochastic moment matching", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'06), pp.638-643, San Jose, CA, March 2006.

C54 J. Shi, Y. Cai, X. Hong, S. X.-D. Tan, "High accurate pattern based precondition method for extremely large power/ground grid analysis", *ACM Symposium on Physical Design* (ISPD'06), pp.108-113, San Jose, CA, April 2006.

C55 A. Kahng, B. Liu, S. X.-D. Tan, "Efficient decoupling capacitor planning via convex programming methods", *ACM Symposium on Physical Design* (ISPD'06), pp.102-107, San Jose, CA, April 2006.

C56 W. Wu, L. Jin, J. Yang, P. Liu and S. X.-D. Tan "A systematic method for functional unit power estimation in microprocessors", *Proc. IEEE/ACM Design Automation Conference* (DAC'06), pp.554-557, CA, 2006.

C57 N. Mi, J. Fan, S. X.-D. Tan, "Statistical analysis of power grid networks considering lognormal leakage current variations with spatial correlation", in *Proc. Int. Conf. Computer Design* (ICCD), pp.56-62, San Jose, CA 2006.

C58 P. Liu, S. X.-D. Tan, B. Yan, B. McGaughy "An extended SVD-based terminal and model order reduction algorithm", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.44-49, San Jose, CA, Sept., 2006.

C59 J. Fan, N. Mi, S. X.-D. Tan, "Variational compact modeling and simulation for linear dynamic systems", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.17-22, San Jose, CA, Sept., 2006.

C60 N. Mi, J. Fan, S. X.-D. Tan, "Simulation of power grid networks considering wires and lognormal leakage current variations", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.73-78, San Jose, CA, Sept., 2006.

C61 B. Yan, S. X.-D. Tan, P. Liu, B. McGaughy, "Passive interconnect macromodeling via balanced truncation of linear systems in descriptor form", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'07), pp. 355-360, Yokohama City, Japan, Jan. 2007.

C62 Y. Zou, Y. Cai, X. Hong, S. X.-D. Tan, "Practical implementation of stochastic

parameterized model order reduction via Hermite polynomial chaos", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'07), pp.367-372, Yokohama City, Japan, Jan. 2007.

C63 L. Kang, Y. Cai, X. Hong, S. X.-D. Tan, "Fast decoupling capacitor budgeting for power/ground networks using random walk approach", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'07), pp.751-756, Yokohama City, Japan, Jan. 2007.

C64 B. Yan, P. Liu, S. X.-D. Tan, B. McGaughy, "Passive modeling of interconnects by waveform shaping", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'07), pp.356-361, San Jose, CA, March 2007.

C65 N. Mi, B. Yan, S. X.-D. Tan, J. Fan, H. Yu "General block structure-preserving reduced order modeling of linear dynamic circuits", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'07), pp. 633-638, San Jose, CA, March 2007.

C66 J. Fan, N. Mi, S. X.-D. Tan, Y. Cai and X. Hong, "Statistical model order reduction for interconnect circuits considering spatial correlations", *Proc. Design, Automation and Test in Europe* (DATE'07), pp. 1508-1513, Nice, France, April 2007.

C67 B. Yan, S. X.-D. Tan, P. Liu, B. McGaughy, "SBPOR: second-order balanced truncation for passive model order reduction of RLC circuits", *Proc. IEEE/ACM Design Automation Conference* (DAC'07), pp.158-161, San Diego, CA, 2007.

C68 N. Mi, S. X.-D. Tan, P. Liu, J. Cui, Y. Cai and X. Hong, "Stochastic extended Krylov subspace method for variational analysis of on-chip power grid networks", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp.48-53, San Jose, CA, Nov. 2007.

C69 D. Li, S. X.-D. Tan, and M. Tirumala, "Architecture-level thermal behavioral modeling for quad-core microprocessors", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp. 22-27, San Jose, CA, Sept., 2007.

C70 J. Fan, G. Yu, J. Tan and S. X.-D. Tan, "Modeling and analysis of biological cells in DRAM implementation", *IEEE International Workshop on Behavioral Modeling and Simulation* (BMAS), pp.90-93, San Jose, CA, Sept., 2007.

C71 J. Fan, N. Mi, S. X.-D. Tan, "Voltage drop reduction for on-chip power delivery considering leakage current variations", in *Proc. Int. Conf. Computer Design* (ICCD), Lake Tahoe, pp. 78-83, CA 2007.

C72 W. Wu, J. Yang, S. X.-D. Tan, S.-L. Lu, "Improving the reliability of on-chip caches under process variations", in *Proc. Int. Conf. Computer Design* (ICCD), Lake Tahoe, pp. 325-332, CA 2007. **Best Paper Award** (<2%).

C73 X. Yuan, J. Fan, B. Liu, S. X.-D. Tan, "Stochastic based extended Krylov subspace method for power/ground network analysis", in *Proc. 7th International Conference on ASIC* (ASICON'07), Guilin, China, Oct. 2007. (**Invited**).

C74 L. Kang, Y. Cai, J. Shi, X. Hong, S. X.-D. Tan, and X. Wang, "Simultaneous switching noise consideration for power/ground network optimization", In *Proc.*

Computer Aided Design &Computer Graphics (CAD&CD'07), Beijing, Oct 2007.

C75 D. Li, S. X.-D. Tan, and M. Tirumala, "Architecture-level thermal behavioral characterization for multi-core microprocessors", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'08), pp.456-461, Seoul, Korea, Jan. 2008.

C76 D. Li, S. X.-D. Tan, "Hierarchical Krylov subspace reduced order modeling of large RLC circuits", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'08), pp.170-175, Seoul, Korea, Jan. 2008.

C77 D. Li, S.X.-D. Tan, B. McGaughy, "ETBR: Extended truncated balanced realization method for on-chip power grid network analysis", *Proc. Design, Automation and Test in Europe* (DATE'08), pp.432-437, Munich, Germany, March 2008.

C78 Z. Luo, S. X.-D. Tan, "Statistic analysis of power/ground networks using single-node SOR method", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'08), pp. 867-872, San Jose, CA, March 2008.

C79 P. Liu, S. X.-D. Tan, W. Wu and M. Tirumala, "FEKIS: A fast architecture-level thermal analyzer for online thermal regulation", *Proc. IEEE/ACM International Great Lakes Symposium on VLSI* (GLSVLSI'08), pp. 411-416, Orlando, 2008.

C80 J. Cui, G. Chen, R. Shen, S. X.-D. Tan, W. Yu, J. Tong, "Variational capacitance modeling using orthogonal polynomial method", *Proc. IEEE/ACM International Great Lakes Symposium on VLSI* (GLSVLSI'08), pp. 23-28, Orlando, 2008.

C81 B. Yan, L. Zhou, S. X.-D. Tan, J. Chen, B. McGaughy, "DeMOR: Decentralized model order reduction of linear networks with massive ports", *Proc. IEEE/ACM Design Automation Conference* (DAC'08), pp. 409-414, Anaheim, CA, 2008.

C82 B. Yan, H. Wang, S. X.-D. Tan, "A survey of RLCK reduction and simulation methods by fast truncated balanced realization", *Int, Conf. Solid State and Integrated Circuit Technology* (ICSICT'08), pp. H1.3, Beijing, China, Oct. 2008. **(invited)**

C83 B. Yan, S. X.-D. Tan, G. Chen, L. Wu, "Modeling and simulation for on-chip power grid networks by locally dominant Krylov subspace method", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp. 744-749, San Jose, CA, Nov. 2008.

C84 D. Li, S. X.-D. Tan, E. H. Pacheco, M. Tirumala, "Parameterized transient thermal behavioral modeling for chip multiprocessors", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp. 611-617, San Jose, CA, Nov. 2008.

C85 W. Zhao, Z. Luo, J. Fan, S. X.-D. Tan, "Vector edge detection in H.264 Implementation", *IEEE 5th International Conference on Embedded Software and Systems Symposia* (ISHSO'08), pp. 208-212, Chengdu, China, July 29-31, 2008.

C86 H. Wang, H. Yu, S. X.-D. Tan, "Fast analysis of non-tree clock network considering environmental uncertainty by parameterized and incremental macromodeling", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'09), pp. 379-384, Yokohama, Japan, Jan. 2009.

C87 D. Li, S. X.-D. Tan, G. Chen and X. Zeng, "Statistical analysis of on-chip power

grid networks by variational extended truncated balanced realization method" *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'09), pp. 272-277, Yokohama, Japan, Jan. 2009.

C88 R. Shen, N. Mi, S. X.-D. Tan, Y. Cai, X. Hong, "Statistical modeling and analysis of chip-level leakage power by spectral stochastic method", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'09), pp. 161-166, Yokohama, Japan, Jan. 2009.

C89 T. Eguia, N. Mi, S. X.-D. Tan, "Statistical decoupling capacitance allocation by efficient numerical quadrature method", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'09), pp. 309-317, San Jose, CA, March 2009.

C90 X. Wang, Y. Cai, S. X.-D. Tan, X. Hong and J. Relles, "An efficient decoupling capacitance optimization using piecewise polynomial models", *Proc. Design, Automation and Test in Europe* (DATE'09), pp.1190--1195, Nice, France, March 2009.

C91 J. Shi, Y. Cai, W. Hou, L. Ma, S. X.-D. Tan, P.-H. Ho and X. Wang, "GPU friendly fast Poisson solver for structured power grid network analysis", *Proc. IEEE/ACM Design Automation Conference* (DAC'09), pp.178--183, San Francisco, CA, 2009. (**Best Paper Award Nomination (7 out of 682 submissions, 1%))**

C92 Z. Luo, J. Fan, S. X.-D. Tan, "Localized statistical 3D thermal analysis considering electro-thermal coupling", *IEEE International Symposium on Circuits and Systems* (ISCAS'09), pp.1289-1292, Taipei, Taiwan, May, 2009.

C93 X. Wang, Y. Cai, Q. Zhou, S. X.-D. Tan and T. Eguia, "Decoupling capacitance efficient placement for reducing transient power supply noise", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), pp. 745-751, San Jose, CA, Nov. 2009.

C94 T. Eguia, S. X.-D. Tan, E. H. Pacheco, M. Tirumala, "Architecture level thermal modeling for multi-core systems using subspace system method", in *Proc. International Conference on ASIC* (ASICON'09), pp. 714-717, Changsha, China, Oct. 2009. (**Invited**).

C95 H. Yu and S. X.-D. Tan, "Recent advance in computational prototyping for analysis of high-performance analog/RF ICs", in *Proc. International Conference on ASIC* (ASICON'09), pp. 760-763, Changsha, China, Oct. 2009 (**invited**).

C96 E. Tlelo-Cuautle, E. Martínez-Romero, C. Sánchez-López, S. X.-D. Tan, "Symbolic formulation method for mixed-mode analog circuits using nullors", In Proc. 16th IEEE International Conference on Electronics, Circuits and Systems (ICECS'09), pp.856-859, Hammamet, Tunisia, Dec. 2009.

C97 H. Yu, X. Liu, H. Wang, S. X.-D. Tan, "A fast analog mismatch analysis by an incremental and stochastic trajectory piecewise linear macromodel", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'10), pp.211-216, Taipei, Taiwan, Jan. 2010.

C98 D. Li, S. X.-D. Tan, N. Mi and Y. Cai, "Efficient power grid integrity analysis using

on-the-fly error check and reduction", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'10), pp.763-768, Taipei, Taiwan, Jan. 2010.

C99 H. Wang, S. X.-D. Tan, G. Chen, "Wideband reduced modeling of interconnect circuits by adaptive complex-valued sampling method", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'10), pp.31-26, Taipei, Taiwan, Jan. 2010.

C100 B. Yan and S. X.-D. Tan, G. Chen, Y. Cai, "Model reduction of interconnects via double gramians approximation", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'10), pp. 25-30, Taipei, Taiwan, Jan. 2010.

C101 T. Eguia, S. X.-D. Tan, R. Shen, E. H. Pacheco, M. Tirumala, "General behavioral thermal modeling and characterization for multi-core microprocessor design", *Proc. Design, Automation and Test in Europe* (DATE'10), Dresden, Germany, pp.1136-1141, March 2010.

C102 R. Shen, S. X.-D. Tan, J. Xiong, "A linear statistical analysis for full-chip leakage power with spatial correlation", *Proc. IEEE/ACM International Great Lakes Symposium on VLSI* (GLSVLSI'10), pp.227-232, Providence, RI, May, 2010.

C103 X. Liu H. Yu, S. X.-D. Tan, "A robust periodic Arnoldi shooting algorithm for efficient large-scale RF/MMIC simulation", *Proc. IEEE/ACM Design Automation Conference* (DAC'10), pp. 573-578, Anaheim, CA, June 2010.

C104 R. Shen, S. X.-D. Tan, J. Xiong, "A linear algorithm for full-chip statistical leakage power analysis considering weak spatial correlation", *Proc. IEEE/ACM Design Automation Conference* (DAC'10), pp.481-486, Anaheim, CA, 2010.

C105 E. Tlelo-Cuautle, E. Martínez-Romero, C. Sánchez-López, S. X.-D. Tan, "Symbolic behavioral modeling of low voltage amplifiers", *IEEE International Conference on Electrical Engineering, Computing Science and Automatic Control* (CCE), México, pp.510-514, September 8-10, 2010.

C106 E. Martínez-Romero, E. Tlelo-Cuautle, C. Sánchez-López, S. X.-D. Tan, "Symbolic noise analysis of low voltage amplifiers by using nullors", *IEEE International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design* (SM2ACD), Tunisia, October 5-6, 2010.

C107 J. Relles, M. Ngan, E. Tlelo-Cuautle, S. X.-D. Tan, C. Hu, W. Yu and Y. Cai, "Statistical extraction and modeling of 3D inductance with spatial correlation", *IEEE International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design* (SM2ACD), Tunisia, October 5-6, 2010.

C108 H. Wang, D. Li, S. X.-D. Tan, M. Tirumala and A. X. Gupta "Composable thermal modeling and characterization for fast temperature estimation", *Conference on Electrical Performance of Electronic Packaging and Systems* (EPEPS), Oct, Austin, TX, 2010.

C109 S. X.-D. Tan, H. Wan, B. Yan, "UiMOR -- UC Riverside model order reduction tool for post-layout wideband interconnect modeling", *Int. Conf. Solid State and Integrated Circuit Technology* (ICSICT'10), Shanghai, China, Oct. 2010. **(invited)**

C110 K. Ma, L. Wang, X. Zhou, S. X.-D. Tan, J. Tong, "General switch box modeling and optimization for FPGA routing architectures", *The 2010 International Conference on Field-Programmable Technology* (FPT'10), Beijing, Dec. 2010.

C111 X. Liu, H. Yu, J. Relles, S. X.-D. Tan, " A structured parallel periodic Arnoldi shooting algorithm for RF-PSS analysis based on GPU platforms", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'11), pp.13-18, Yokohama, Japan, Jan. 2011.

C112 Z. Hao, R. Shen, S. X.-D. Tan, B. Liu, G. Shi and Y. Cai, "Statistical full-chip dynamic power estimation considering spatial correlations", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'11), San Jose, CA, pp677-782, March 2011.

C113 Z. Hao, S. X.-D. Tan, G. Shi, "An efficient statistical chip-level total power estimation method considering process variations with spatial correlation", *Proc. Int. Symposium. on Quality Electronic Design* (ISQED'11), pp.671-676, San Jose, CA, March 2011.

C114 J. Lu, Z. Hao, S. X.-D. Tan, "Graph-based parallel analysis of large analog circuits based on GPU platforms", *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU Workshop), Santa Barbara, CA, April 2011.

C115 Z. Hao, S. X.-D. Tan, R. Shen, G. Shi, "Performance bound analysis of analog circuits considering process variations", *Proc. IEEE/ACM Design Automation Conference* (DAC'11) , pp.310-315, San Diego, CA, June 2011.

C116 Z. Liu, S. X.-D. Tan, H. Wang, R. Quintanilla and A. Gupta, "Compact thermal modeling for package design with practical power maps", *1st International IEEE Workshop on Thermal Modeling and Management: Chips to Data Centers* (TEMM), Orlando, FL, July, 2011.

C117 Z. Liu, S. X.-D. Tan, H. Wang, R. Quintanilla and A. Gupta, "Compact behavioral thermal modeling for microprocessor design with spatially correlated power inputs", *TECHCON'2011* , Austin, TX, Sept. 2011.

C118 H. Wang, S. X.-D. Tan, G. Liao, R. Quintanilla and A. Gupta, "Full-chip runtime error-tolerant thermal estimation and prediction for practical thermal management", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD), San Jose, CA, pp.716-723, Nov. 2011.

C119 S. Swarup, S. X. -D. Tan, Z. Liu, H. Wang, Z. Hao and G. Shi, "Battery state of charge estimation using adaptive subspace identification method", in *Proc. International Conference on ASIC* (ASICON'11), Xiamen, China, Oct. 2011.

C120 X. Liu, S. X.-D. Tan, Z. Hao, G. Shi, "Time-domain performance bound analysis of analog circuits considering process variations", ", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'12), Sydney, Australia, pp.535-540, Jan. 2012.

C121 X. Liu, S. X.-D. Tan, H. Wang and H. Yu, "A GPU-accelerated envelope-following method for switching power converter simulation", *Proc. Design, Automation and Test in Europe* (DATE'12), pp.1349-1354, Dresden, Germany,

March 2012.

C122 X. Liu, S. X.-D. Tan, and H. Wang, "Parallel statistical analysis of analog circuits by GPU-accelerated graph-based approach", *Proc. Design, Automation and Test in Europe* (DATE'12), pp.852-857, Dresden, Germany, March 2012.

C123 H. Wang, S. X.-D. Tan, X. Liu, A. Gupta, "Runtime power estimator calibration for high-performance microprocessors", *Proc. Design, Automation and Test in Europe* (DATE'12), pp.352-357, Dresden, Germany, March 2012.

C124 X. Liu, Z. Liu, S. X.-D. Tan, J. Gordon, "Full-chip thermal analysis of 3D ICs with liquid cooling by GPU-accelerated GMRES method", *Proc. Int. Symposium on Quality Electronic Design* (ISQED'12), San Jose, CA, March 2012.

C125 R. Shen, S. X.-D. Tan and X. Liu, "A new voltage binning technique for yield improvement based on graph theory", *Proc. Int. Symposium on Quality Electronic Design* (ISQED'12), San Jose, CA, March 2012.

C126 S. Rodriguez-Chavez , E. Tlelo-Cuautle, A. Palma-Rodriguez, S. X.-D. Tan, "Symbolic DDD-based tool for the computation of noise in CMOS analog circuits", *8th International Caribbean Conf. on Devices, Circuits and Systems* (ICCDCS), Playa del Carmen, Mexico, March 2012.

C127 A. Palma-Rodriguez, S. Rodriguez-Chavez , E. Tlelo-Cuautle, S. X.-D. Tan, "DDD-based symbolic sensitivity analysis of active filters", *8th International Caribbean Conf. on Devices, Circuits and Systems* (ICCDCS), Playa del Carmen, Mexico, March 2012.

C128 X. Liu, S. X.-D. Tan, Z. Liu, H. Wang, T. Xu, "Transient analysis of large linear dynamic networks on hybrid GPU-multicore platforms", *10th IEEE International NEWCAS Conference*, Montreal, Canada, pp. 173-176, June, 2012.

C129 E. Tlelo-Cuautle, C. Sánchez-López, S. X.-D. Tan, "Symbolic nodal analysis of analog circuits using pathological elements", *10th IEEE International NEWCAS Conference*, Montreal, Canada, pp. 161-164, June, 2012.

C130 R. Li and Y. Shi and S. X.-D. Tan, "The fast convergence analysis of finite-time consensus for multi-agent systems with switching topology", *Proc. 31th Chinese Control Conference*, July 2012.

C131 Z. Liu, S. X.-D. Tan, H. Wang, Y. Hua, and A. Gupta, "Compact nonlinear thermal modeling of packaged microprocessors", *TECHCON'2012* , Austin, TX, Sept. 2012.

C132 S. Xu, Y. Hua, and S. X.-D. Tan, "Thermal modeling and temperature prediction using least square model averaging with model screening", *TECHCON'2012* , Austin, TX, Sept. 2012.

C133 S. Swarup, S. X.-D. Tan, and Z. Liu, "Thermal characterization of TSV based 3D stacked ICs", *Conference on Electrical Performance of Electronic Packaging and Systems* (EPEPS), Oct, Tempe, AZ, 2012.

C134 Z. Liu, T. Xu, S. X.-D. Tan, and H. Wang, "Dynamic thermal management for multi-core microprocessors considering transient thermal effects", *Proc. Asia South*

Pacific Design Automation Conference (ASP-DAC'13), pp.473-478, Yokohama, Japan, Jan. 2013.

C135 X. Liu, A. Palma-Rodriguez , S. Rodriguez-Chavez, S. X.-D. Tan, E. Tlelo-Cuautle, Y. Cai, "Performance bound and yield analysis for analog circuits under process variations", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'13), pp.761-766, Yokohama, Japan, Jan. 2013.

C136 Z. Liu, S. X.-D. Tan, H. Wang, A. Gupta, and S. Swarup , "Compact nonlinear thermal modeling of packaged integrated systems", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'13), pp.157-162, Yokohama, Japan, Jan. 2013.

C137 H. Wang, S. X.-D. Tan, S. Swarup, and X. Liu, "A power-driven thermal sensor placement algorithm for dynamic thermal management", *Proc. Design, Automation and Test in Europe* (DATE'13), pp.1215-1220, Grenoble, France, March 2013.

C138 Z. Liu, S. Swarup, and S. X.-D. Tan, "Compact lateral thermal resistance modeling and characterization for TSV and TSV array", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'13), pp.275-280, San Jose, CA, Nov. 2013.

C139 X. Liu, H. Wang, and S. X.-D. Tan, "Parallel power grid analysis using preconditioned GMRES solvers on CPU-GPU platforms", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'13), pp.561-568, San Jose, CA, Nov. 2013.

C140 Z. Liu, X. Huang, S. X.-D. Tan, H. Wang, H. Tang, "Distributed task migration for thermal hot spot reduction in many-core microprocessors", in *Proc. International Conference on ASIC* (ASICON'13), Shenzhen, China, Oct. 2013. (**Invited**).

C141 T. Yu, S. X.-D. Tan, Y. Cai, and P. Tang, "Time-domain performance bound analysis for analog and interconnect circuits considering process variations", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'14), Singapore, Singapore, Jan. 2014.

C142 Y. Chi, S. X.-D. Tan, T. Yu, X. Huang and N. Wong, "Direct finite-element-based solver for 3D-IC thermal analysis via H-matrix representation", *Proc. Int. Symposium on Quality Electronic Design* (ISQED'14), San Jose, CA, March, 2014.

C143 X. Huang, T. Yu, V. Sukharev, S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks", *Proc. IEEE/ACM Design Automation Conference* (DAC'14), San Francisco, June, 2014. (**Best Paper Award Nomination (12 out of 787 submissions, 1.5%))**

C144 T. Wei, T. Kim, S. Park, Q. Zhu, S. X.-D. Tan, N. Chang, S. Ula, M. Maasoumy , "Battery management and application for energy-efficient buildings", *Proc. IEEE/ACM Design Automation Conference* (DAC'14), San Francisco, June, 2014.

C145 K. He, S. X.-D. Tan, E. Tlelo-Cuautle, H. Wang and H. Tang, "A new segmentation-based GPU-accelerated sparse matrix-vector multiplication", *Proc. Int. Midwest Symposium on Circuits and Systems* (MWSCAS'14), College Station,

TX, August, 2014.

C146 Z. Liu, X. Huang, V. Sukharev and S. X.-D. Tan, "EM-reliability system modeling and performance optimization for high-performance microprocessors", *TECHCON'2014* , Austin, TX, Sept. 2014.

C147 A. Zhang, G. Shi, S. X.-D. Tan, J. Cheng, "Simultaneous SNR and SNR-variation optimization for Sigma-Delta modulator design", *Int, Conf. Solid State and Integrated Circuit Technology* (ICSICT'04), Guilin, China, Oct. 2014. (**invited**)

C148 V. Sukharev, X. Huang, H. Chen and S. X.-D. Tan, "IR-drop based electromigration assessment: parametric failure chip-scale analysis", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'14), San Jose, CA, Nov. 2014.

C149 T. Kim, B. Zheng, H. Chen, Q. Zhu, V. Sukharev and S. X.-D. Tan, "Lifetime optimization for real-time embedded systems considering electromigration effects" *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'14), San Jose, CA, Nov. 2014.

C150 J. Ma, H. Wang, S. X.-D. Tan, C. Zhang, H. Tang, "Hybrid dynamic thermal management method with model predictive control*", IEEE Asia Pacific Conference on Circuit and Systems (APCCAS'14)*, Ishigaki Island, Okinawa, Japan, Nov. 2014.

C151 Y. Zhu, S. X.-D. Tan, "GPU-accelerated parallel Monte Carlo analysis of analog circuits by hierarchical graph-based solver"*, Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'15), Chiba, Japan, Jan. 2015.

C152 H. Chen, S. X.-D. Tan, X. Huang, V. Sukharev, "New electromigration modeling and analysis considering time-varying temperature and current densities", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'15), Chiba, Japan, Jan. 2015. (**Best Paper Award Nomination, 7 out of 318)**

C153 H. Shin, S. X.-D. Tan, G. Shi and E. Tlelo-Cuautle, "Rare event diagnosis by iterative failure region locating and elite learning sample selection", *Latin-American Test Symposium* (LATS), Puerto Vallarta, Mexico, March, 2015.

C154 H. Chen, X. Huang, V. Sukharev, S. X.-D. Tan and T. Kim, "Interconnect reliability modeling and analysis for multi-branch interconnect trees", *Proc. IEEE/ACM Design Automation Conference* (DAC'15), San Francisco, June, 2015.

C155 T. Kim, X. Huang, V. Sukharev and S. X.-D. Tan, "A dynamic reliability management framework for dark silicon", *TECHCON'2015*, Austin, TX, September 2015.

C156 Y. Zhao, H. Shin, H. Chen, S. X.-D. Tan, G. Shi, X. Li, "Statistical rare event analysis using smart sampling and parameter guidance", *28th IEEE International SoC Conference* (SOCC2015), Beijing, Sept, 2015.

C157 X. Huang, V. Sukharev, J.-H. Choy, H. Chen, E. Tlelo-Cuautle and S. X.-D. Tan, "Full-chip electromigration assessment: effect of cross-layout temperature and thermal stress distributions", *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD),

Istanbul, Turkey, Sept. 2015.

C158 T. Kim and X. Huang, V. Sukharev, S. X.-D. Tan, "Learning-based reliability management for dark silicon systems", *6th IEEE International Workshop on Testing 3D Stacked ICs* (3D-Test), Anaheim, CA, Oct., 2015.

C159 K. He, X. Huang, S. X.-D. Tan, "EM-based on-chip aging sensor for detection and prevention of counterfeit and recycled ICs"*, Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'15), Austin, TX, Nov. 2015.

C160 H. Zhao, D. Quach, S. Wang, H. Wang, H. Chen, X. Li and S. X.-D. Tan, "Learning based compact thermal modeling for energy-efficient smart building management", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'15), Austin, TX, Nov. 2015. (**invited**)

C161 X. Chen, X. Li and Sheldon X.-D. Tan, "From robust chip to smart building: CAD Algorithms and methodologies for Uncertainty Analysis of Building Performance", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'15), Austin, TX, Nov. 2015. (**invited**)

C162 X. Huang, V. Sukharev, T. Kim, H. Chen and S. X.-D. Tan, "Electromigration recovery modeling and analysis under time-dependent current and temperature stressing"*, Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'16), Macao, China, Jan. 2016.

C163 W. Liu, H. Wang, H. Zhao, S. Wang, H. Chen, Y. Fu, J. Ma, X. Li, S. X.-D. Tan, "Thermal modeling for energy-efficient smart building with advanced overfitting mitigation technique", *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC'16), Macao, China, Jan. 2016. (**invited**)

C164 T. Kim, X. Huang, H. Chen, V. Sukharev and S. X.-D. Tan, "Learning-based dynamic reliability management for dark silicon processor considering EM effects", *Proc. Design, Automation and Test in Europe* (DATE'16), Dresden, Germany, March 2016.

C165 L. Zhang, H. Wang and S. X.-D. Tan, , "Fast stress analysis for runtime reliability enhancement of 3D IC using artificial neural networks", *Proc. Int. Symposium on Quality Electronic Design* (ISQED'16), San Jose, CA, March, 2016.

C166 X. Chen, X. Li and S. X.-D. Tan, "Overview of cyber-physical temperature estimation in smart buildings: from modeling to measurements", *IEEE INFOCOM Workshop on Cross-Layer Cyber Physical Systems Security* (CPSS), San Francisco, CA, April, 2016.

C167 H. Zhao, Z. Qi, S. Wang, K. Vafai, H. Wang, H. Chen, S. X.-D. Tan, "Learning-based occupancy behavioral detection for smart buildings", *Proc. IEEE International Symposium on Circuits and Systems* (ISCAS), Montreal, Canada, May, 2016.

C168 X. Huang, V. Sukharev, Z. Qi, T. Kim and S. X.-D. Tan, "Physics-based full-chip TDDB assessment for BEOL Interconnects", *Proc. IEEE/ACM Design Automation Conference* (DAC'16), Austin, TX, June, 2016.

C169 T. Kim, Z. Sun, C. Cook, H. Zhao, R. Li, D. Wong and S. X.-D. Tan, "Cross-layer modeling and optimization for electromigration induced reliability", *Proc. IEEE/ACM Design Automation Conference* (DAC'16), Austin, TX, June 2016. (**Invited**)

C170 C. Cook, Z. Sun, T. Kim and S. X.-D. Tan, "Finite difference method for electromigration analysis of multi-branch interconnects", *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD'16), Lisbon, Portugal, June 2016.

C171 H. Wang, M. Zhang, S. X.-D. Tan, C. Zhang, Y. Yuan, K. Huang and Z. Zhang, "New power budgeting and thermal management scheme for multi-core systems in dark silicon", *29th IEEE International SoC Conference* (SOCC'16), Seattle, WA Sept, 2016.

C172 C. Cook, Z. Sun, T. Kim and S. X.-D. Tan, "Finite difference time domain analysis of stress evolution and void growth for general interconnect wires", *TECHCON'2016*, Austin, TX, September 2016.

C173 H. Zhao, S. X.-D. Tan, H. Wang, H. Chen, "Online unusual behavior detection for temperature sensor networks", *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'16)*, pp. 59-62, Pittsburg, PA, Sept. 2016.

C174 X. Chen, H. Chen, W. Ma, X. Li, S. X.-D. Tan, "Energy-efficient wireless temperature sensoring for smart building application*", Int, Conf. Solid State and Integrated Circuit Technology (ICSICT'16)*, Hangzhou, China, Oct. 2016. **(invited)**

C175 Z. Sun, E. Demircan, M. Shroff, T. Kim, X. Huang, S. X.-D. Tan, "Voltage-based electromigration immortality check for general multi-branch interconnects", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'16), Austin, TX, Nov. 2016.

C176 T. Kim, Z. Sun, J. Gaddipati, H. Wang, H. Chen, S. X.-D. Tan, "Dynamic reliability management for near-threshold dark silicon processors", *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD'16), Austin, TX, Nov. 2016. (**Invited**)

C177 L. Xu, H. Wang, S. X.-D. Tan, C. Zhang, Y. Yuan, K. Huang, Z. Zhang, "Distributed model predictive control for dynamic thermal management of multi-core systems", *Int., Conf. Solid State and Integrated Circuit Technology (ICSICT'16)*, Hangzhou, China, Oct. 2016.

C178 J. Wan, H. Wang, J. He, S. X.-D. Tan, Y. Cai, S. Yang "A fast full-chip static power estimation method", *Int., Conf. Solid State and Integrated Circuit Technology (ICSICT'16)*, Hangzhou, China, Oct. 2016.

C179 S. Wang, H. Zhao, S. X.-D. Sheldon Tan and M. Tahoori, "Recovery-aware proactive TSV repair for electromigration in 3D ICs", *Proc. Design, Automation and Test in Europe* (DATE'17), Lausenne, Switzerland, March 2017.

C180 X. Wang, H. Wang, J. He, S. X.-D. Tan, Y. Cai and S. Yang, "Physics-based

electromigration modeling and assessment for multi-segment interconnects in power grid networks", *Proc. Design, Automation and Test in Europe* (DATE'17), Lausanne, Switzerland, March 2017.